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# UNITED STATES DISTRICT COURT NORTHERN DISTRICT OF CALIFORNIA SAN FRANCISCO DIVISION

3COM CORPORATION,

Plaintiff/Counterdefendant,

V.

D-LINK SYSTEMS INC.,

and

REALTEK SEMICONDUCTOR CORPORATION

Defendants/Counterplaintiffs.

Case No. Cv-03-2177-VRW

JOINT CLAIM CONSTRUCTION AND PRE-HEARING STATEMENT PURSUANT TO PATENT LOCAL RULE 4-3

Plaintiff/Counterdefendant 3Com Corporation and Defendants/Counterplaintiffs
Realtek Semiconductor Corporation and D-Link Systems Inc., by and through respective counsel,
hereby respectfully submit the following Joint Claim Construction and Pre-Hearing Statement
pursuant to Patent L.R. 4-3 of the United States District Court for the Northern District of
California.

The parties exchanged proposed terms and claim elements for construction pursuant to Patent L.R. 4-1. The parties thereafter exchanged proposed constructions for each term and claim element pursuant to Patent L.R. 4-2 and conducted a meet-and-confer conference regarding the proposed terms and claim elements. The parties expressly reserve their rights to propose constructions of additional terms, phrases or clauses in the asserted patents at a later time. In addition, the parties expressly reserve their rights to supplement or amend the proposed construction and other positions set forth herein.

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## I. <u>PATENT L.R. 4-3(a): CLAIM TERMS, PHRASES, OR CLAUSES ON WHICH THE PARTIES AGREE</u>

Pursuant to Patent L.R. 4-3(a), the parties identify those claim terms, phrases, or clauses on which they agree:

### A. Claim Terms not Asserted by Parties as Subject to Construction According to 35 U.S.C. § 112 ¶ 6

6	Claim town	Laint construction
_ ا	Claim term "buffer"	Joint construction  A memory for temporary storage of data
/∥	buller	71 memory for temporary storage of data
8	agreed to with respect to:	
9	'625 patent: 23	
10	'884 patent: 1	
11	The definition of buffer remains in dispute with respect to:	
12	'459 patent: 1	
13	'872 patent: 1, 10, 21	
14	'094 patent: 1, 9, 21, 28, 39, 47	A coming on third constant (COMA) with collision datastic (CD) at 1
15	"CSMA/CD"	A carrier sense multiple access (CSMA) with collision detection (CD) network, such as an Ethernet network
	found in claim numbers:	Such as an Exherite network
16	'872 patent: 21	
17	'094 patent: 28	
18	"carrier sense, multiple access	A carrier sense multiple access (CSMA) with collision detection (CD) network,
	network with collision detection"	such as an Ethernet network
19	found in claim numbers:	
20	'872 patent: 21	
21	'094 patent: 28	
22	"coupled to the first and second ports"	connected
23	found in claim numbers:	
24	'625 patent: 23	
25	"frame(s)"	A bundle of data in binary form organized in a specific way for transmission
26	found in claim numbers:	
27	'459 patent: 1	
- 11		

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1	Claim term	Joint construction
2	'872 patent: 1, 10, 21	
_	'094 patent:1, 9, 21, 28, 39, 47	
3	"in parallel"	A period of concurrent operation
4	found in claim numbers:	
5	'094 patent: 1, 39	
	"medium access controller"	A device that controls access to the network
6	found in claim numbers:	
/	'872 patent: 21	
8	"medium access task"	A task performed by a network interface device for initiating access to a
9	found in claim numbers:	network
10	'094 patent: 39 "monitoring"	
10	"monitoring"	Watching, keeping track of, or checking on
11	found in claim numbers:	
12	'094 patent: 9, 21, 28, 39	
13	'872 patent: 1, 10	
14	"network interface adapter"	Equipment between a computer and a network for enabling communication
15	found in claim numbers:	
16		
10	'872 patent: 21	
17	"order of receipt"	The order in which the packets are received by the buffer
18	found in claim numbers:	
19	'625 patent: 23	
17	"packet filter"	Hardware and/or software that identifies packets as having variant formats
20	found in claim numbers:	
21	'884 patent: 1	
22	"port"	An access point for data entry or exit
23	found in claim numbers:	
24	'625 patent: 23	
25	'884 patent: 1	
دے	"posting status information"	Storing information about the state of a function or operation
26	found in claim numbers:	
27	'872 patent: 10	
	<u> </u>	

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1						
1	Claim term	Joint construction				
2	'094 patent: 21, 47					
3	"produce a data value dependent on contents of the packet prior to transfer of the identified packets"	Produce a data value dependent on the contents of the packet before transferring the identified packets to the host				
4	found in claim numbers:					
5	'884 patent: 1					
6	"segmentation circuit"	Circuitry that generates the frame segment descriptor utilizing the descriptor signal				
7	found in claim numbers:					
8	'446 patent: 26 "threshold determination"	A determination of whether the threshold amount has been reached				
9	found in claim numbers:					
10	'872 patent:1, 10, 21					
11	'094 patent: 9, 28, 47					
12	"threshold logic"	Circuits and/or programming that determine(s) whether the threshold value has been reached				
13	found in claim numbers:					
14	'459 patent: 1 "transceiver"	A device that can both transmit and receive signals				
15	found in claim numbers:					
16	'459 patent: 1					
17	'872 patent: 10					
18	'094 patent: 28 "transfer packets out of the buffer	The order in which packets are transferred out of the buffer is based upon the				
19	to the other of the first and second ports according to the order of	order in which the packets were received by the buffer and the types of the packets stored in the buffer				
20	receipt, and according to the respective packet types"					
21	found in claim numbers:					
22	'625 patent: 23					
23						

#### II. PATENT L.R. 4-3(b): DISPUTED CLAIM TERMS, PHRASES AND CLAUSES

Pursuant to Patent L.R. 4-3(b), the parties identify the following claim terms, phrases, or clauses on which they disagree, and submit these terms for construction by the Court:

25

## A. Claim Terms not Asserted by Parties as Subject to Construction According to 35 U.S.C. § 112 ¶ 6¹

#### 1. <u>U.S. Pat. No. 5,307,459</u>

- 11				
	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
4	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
		evidence	evidence	evidence
5	"alterable storage	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
	location"	storage location whose	storage location whose	storage location whose
6		value is changeable	value is dynamically	value is dynamically
Ĭ	found in claim		changeable	changeable
7	numbers:	DICTIONARY/TREATISE	3.4.5	<i>3</i>
′∥		DEFINITIONS:	INTRINSIC EVIDENCE:	INTRINSIC EVIDENCE:
8	'459 patent: 1	alter: The American		
O	. · · ·	Heritage Dictionary of the	PATENT SPECIFICATION:	'459 patent at 42:17-25
		English Language (4th ed.		("The above indication
9		2000): v. tr. To change or	"If host processor 5	signals are further
1.0		make different; modify:	responds to network adapter	optimized by allowing the
10		altered my will. intr. To	3 before a complete data	host processor to
		change or become different.	frame is transferred, host	dynamically tune the timing
11			processor 5 then may	of the indication signals.
		INTRINSIC EVIDENCE:	decrease the threshold value	The host processor has write
12		Claims: see, e.g., claim 5	in alterable storage location	access to the threshold
		(depending from claim 1,	10a enabling threshold logic	registers and may alter the
13		claim 5 claiming posting	10 to generate the indication	threshold values in the
		status information which	signal at a later time in the	threshold registers based on
14		may be used by the host	next transfer of a data	posted status information by
		processor as feedback);	frame. Alternatively, if host	the network adapter. The
15		claim 1; claim 7, claim 22;	processor 5 responds to the	posted status information
		claim 23; claim 34; claim	network adapter 3 after a	will <i>allow the host</i>
16		35; claim 40; claim 41;	complete data frame has	processor to determine
10		claim 44; claim 45; claim	already been transferred,	whether it is responding too
17		50; claim 51; claim 52;	host processor 5 may then	early or too late to an
1 /		claim 53; Specification: see,	increase the threshold value	interrupt generated by the
18		e.g., fig. 2, 14-24; col. 2:47-	in alterable storage location	indications.")
10		50 ("The threshold logic	10a enabling the threshold	marcanons.
19		includes a counter coupled	logic to generate an	'459 patent at 6:31-59
19		to the buffer memory for	indication signal at an	("Threshold logic 10
20		counting the data transfer to	earlier time in the next	contains an alterable
20		or from the buffer memory,	transfer of a data frame."	storage location 10a which
		and an alterable storage	('459; Col. 6: 48-59).	contains a threshold value.
21		location containing a	(133, 601. 0. 10 33).	This threshold value
		threshold value."); 3:8-14	"The above indication	represents the amount of a
22		("According to another	signals are further optimized	data frame which will be
		aspect of the present	by allowing the host	transferred into or out of
23		invention, the network	processor to dynamically	buffer 9 before an early
		interface logic includes	tune the timing of the	indication signal will be
24		interface regie merades	tane the thining of the	maieution signar will be

<sup>&</sup>lt;sup>1</sup> Defendants contend that "logic" is a signal which invokes 35 U.S.C. § 112 ¶6 in certain asserted claims, while Plaintiff contends that it is an ordinary term. "Logic," and various phrases beginning with that term, are included in this section either because all parties have proposed constructions or because one or more defendants proposed the phrase for construction not under § 112 ¶6 in its 4-1 statement, and because the dispute with respect to whether the term invokes 35 U.S.C. § 112 ¶6 is adequately noted in Sections B and D.

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
1	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2	(wisputed terms in outl)	evidence	evidence	evidence
		control means for	indication signals. The host	generated which may cause
3		generating an interrupt	processor has write access	host interface logic 8 to
		signal to the host processor	to the threshold registers	send an interrupt to host
4		responsive to the indication	and may alter the threshold	processor 5
		signal. The control means	values in the threshold	
5		also posts status information	registers based on posted	The threshold logic also
		which may be used by the	status information by the	includes a means for the
6		host processor as feedback	network adapter. The	host processor 5 to
		for optimizing the threshold	posted status information	dynamically alter the time at which an indication is
7		value in the alterable storage location."); see also col.	will allow the host processor to determine whether it is	generated based on prior
		2:50-54; col. 3:18-25; col.	responding too early or too	host processor 5 responses.
8		3:37-56; col. 3:67-4:2; col.	late to an interrupt generated	When responding to an
		4:7-11; col. 6:32-33; col.	by the indications." ('459;	interrupt generated by an
9		6:38-59; col. 23:56-59; col.	Col. 42: 17-25) (emphasis	early indication, the host
$\ $		29:64-67; col. 30:45-48; col.	added).	processor may examine
10		31:20-22; col. 42:19-22;		network adapter status
, ,		Col. 1: 46-51; Col. 1: 63-66;	"The control means also	information to determine if
11		Col. 2: 46-54; Col. 2: 30-35;	posts status information	host processor 5 is servicing
12		Col. 2: 23-27; Col. 6: 9-59;	which may be used by the	the interrupt too early or too
14		Col. 41:44-55; Col. 3:11-14;	host processor as feedback	late. If host processor 5
13		42: 17-25; Col. 6: 48-59;	for optimizing the threshold	responds to network adapter
13		Col. 6:31-59; Col. 42:17- 25; see also Prosecution	value in the alterable storage location." ('459; Col. 3: 11-	3 before a complete data frame is transferred, host
14		History: Notice of	14) (emphasis added).	processor 5 then may
17		Allowability, Oct. 14, 1993,	(emphasis added).	decrease the threshold value
15		pp. 2-3.	"Threshold logic 10 in	in alterable storage location
1		TT.	network adapter 3 is	10a enabling threshold logic
16		EXTRINSIC EVIDENCE:	designed for eliminating or	10 to generate the indication
		3Com's expert, Dr. Michael	reducing interrupt latency.	signal at a later time in the
17		Mitzenmacher may provide	Threshold logic 10 makes a	next transfer of a data
		an expert report or other	determination of how much	frame. Alternatively, if host
18		form of testimony regarding	of a data frame is	processor 5 responds to the
		the technology to which this	transferred before	network adapter 3 after a
9		term relates and how a	generating an early	complete data frame has
		person having ordinary skill in the art in the field of	indication signal. The early indication signal may then	already been transferred, host processor 5 may then
20		networking technology	cause an early interrupt	increase the threshold value
		would understand this term.	signal to be generated	in alterable storage location
21		3Com reserves the right to	during the transfer of a data	10a enabling the threshold
$\ $		rely on testimony by any	frame. Moreover, threshold	logic to generate an
22		expert in this action.	logic 10 is designed such	indication signal at an
$\ _{c_{\lambda}}\ $			that the time required for	earlier time in the next
23		See also U.S. Patent Nos.	transferring the remainder	transfer of a data frame.")
ر ٍ ا		5,434,872; 5,732,094;	of the data frame should	
24		6,327,625; 6,526,446; and	approximately equal the	(450 )
, [		6,570,884; Joint Claim	time required for host	'459 patent at 3: 11-14
25		Construction Statement in	processor 5 save its system	("The control means also
26		Cv-05-00098 (VRW).	parameters. Therefore, interrupt latency is	posts status information which may be used by the
-0		2Com regeries the minute.	eliminated or reduced by	host processor as feedback
$_{27}$		3Com reserves the right to rely on any statement made	allowing host processor 5's	for optimizing the threshold
- '		Tory on any statement made	interrupt routine to coincide	value in the alterable storage
28		1	1	
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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supportin
- /	evidence	evidence with the transfer of the	evidence location.")
	by any party under the Patent Local Rules.	remainder of the data frame.	location.
		FIG. 2 is a functional block	'459 patent at 41: 44-55
		diagram of network adapter	("Therefore, the present
		3 with threshold logic 10	invention reduces host
		illustrating the various transfer paths. Network	processor interrupt latency by generating early
		adapter 3 contains	indications of data frame
		transceiver 12 which	transfers. These early
		transmits and receives data	indications then may be
		frames across network 2.	used to generate an early
		Network interface logic 11	interrupt to the host
		is responsible for the transfer of a data frame	processor before the data frame is transferred which
		between network buffer 9	allows the host processor to
		and transceiver 12.	save its current environment
		Likewise, the network	during a data frame transfe
		adapter 3 contains host	")
		interface logic 8 which is responsible for transferring	DICTIONARY/TREATISE
		a data frame between	DEFINITIONS:
		network buffer 9 and host	ZZIIIIIOIIO.
		system 1. Threshold logic	Webster's Ninth New
		10 contains an alterable	Collegiate Dictionary (Nin
		storage location 10a which	Edition, 1988)
		contains a threshold value. This threshold value	Alter: 1: to make different without changing into
		represents the amount of a	something else
		data frame which will be	2: CASTRATE SPAY ~ v
		transferred into or out of	to become different syn see
		buffer 9 before an early	CHANGE; alterable – adj.
		indication signal will be generated which may cause	EXPERT TECTIMONIA:
		host interface logic 8 to	EXPERT TESTIMONY:
		send an interrupt to host	Realtek's expert, Dr. Izhak
		processor 5. Host processor	Rubin, may provide
		5 has access to the alterable	testimony as to the
		storage 10a location containing the threshold	definition of the disputed terms as would be
		value through host interface	understood by one of
		logic 8. The threshold logic	ordinary skill in the relevan
		also includes a means for	art and may provide an
		the host processor 5 to	explanation of the
		dynamically alter the time at which an indication is	technology.
		generated based on prior	
		host processor 5 responses.	
		When responding to an	
		interrupt generated by an	
		early indication, the host	
		processor may examine network adapter status	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supportin
	evidence	evidence	evidence
		host processor 5 is servicing	
		the interrupt too early or too	
		late. If host processor 5	
		responds to network adapter	
		3 before a complete data	
		frame is transferred, host	
		processor 5 then may	
		decrease the threshold value	
		in alterable storage location	
		10a enabling threshold logic	
		10 to generate the indication	
		signal at a later time in the	
		next transfer of a data	
		frame. Alternatively, if host	
		processor 5 responds to the	
		network adapter 3 after a	
		complete data frame has	
		already been transferred,	
		host processor 5 may then	
		increase the threshold value	
		in alterable storage location	
		10a enabling the threshold	
		logic to generate an	
		indication signal at an earlier time in the next	
		transfer of a data frame."	
		('459; Col. 6: 9-59)	
		(emphasis added).	
		"Therefore, the present	
		invention reduces host	
		processor interrupt latency	
		by generating early	
		indications of data frame	
		transfers. These early	
		indications then may be	
		used to generate an early	
		interrupt to the host	
		processor before the data	
		frame is transferred which	
		allows the host processor to	
		save its current environment	
		during a data frame transfer.	
		The early indications are	
		generated by threshold logic	
		which determines how	
		much of a data frame is	
		transferred before	
		generating an early	
		indication by comparing a	
		threshold value in a	
		threshold register to a data	
	•	transfer counter." ('459;	i .

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
	evidence	evidence   Col. 41: 44-55).	evidence
		·	
		"Therefore, it is desirable to provide a network adapter	
		with an optimized indication	
		signal to the host processor	
		of the completion of the transfer of a data frame	
		which reduces interrupt	
		latency allowing for	
		optimized network adapter/host system	
		performance." ('459; Col.	
		2: 23-27).	
		"The present invention	
		provides for optimized indication signals to a host	
		processor by a network	
		adapter of the completion of	
		a transfer of a data frame. The apparatus is coupled	
		between a network	
		transceiver and a host	
		system which includes a host processor and host	
		memory.").	
		"The threshold logic	
		includes a counter coupled	
		to the buffer memory for counting the data transfer to	
		or from the buffer memory,	
		and an alterable storage location containing a	
		threshold value. Means for	
		comparing the counter and	
		the alterable storage location is also provided.	
		The indication signal to the	
		host is generated based on	
		the comparison of the counter and the threshold	
		value in the alterable storage	
		location." ('459; Col. 2: 46-54).	
		"As can be seen, there is interrupt latency between	
		when the network adapter	
		has completed a transfer and	
		when the host processor is able to service the interrupt	

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
	- Critical Control	generated by the network adapter." ('459; Col. 1: 63-66).	Critical
		"In prior art systems, such as the National	
		Semiconductor DP83932B, a systems-oriented network interface controller	
		(SONIC) and the Intel 82586 local area network co-processor, an interrupt is	
		generated by the network adapter to the host processor	
		on the completion of a data transfer." ('459; Col. 1: 46-51).	
		EXTRINSIC EVIDENCE:	
		DICTIONARY/TREATISE DEFINITIONS:	
		Webster's II New College Dictionary (2001), pg. 33:	
		Alterable-"Capable of being changed."	
		EXPERT TESTIMONY:	
		D-Link's expert, Howard Frazier, may provide testimony as to the	
		definition of the disputed terms as would be	
		understood by one of ordinary skill in the relevant art and may provide an	
		explanation of the technology.	
		D-Link also incorporates by reference Realtek's	
"buffer"	PROPOSED CONSTRUCTION:	references. PROPOSED CONSTRUCTION:	Same as "buffer memory"
found in claim	A memory for temporary storage of data.	This term is used only in phrase "buffer memory."	identified below.
numbers:	DICTIONARY/TREATISE	See construction of "buffer memory."	
'459 patent: 1	DEFINITIONS: The American Heritage Dictionary of the		
also presented for	English Language (4th ed.		

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
1	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2	(aispuied terms in <b>botu</b> )	evidence	evidence	evidence
		used to store data		
3	'872 patent: 1, 10, 21	temporarily; see also		
		<u>Dictionary of Computing</u>		
4	'094 patent: 1, 9, 21,	(3d ed. 1990): A temporary		
	28, 39, 47	memory for data, normally		
5		used to accommodate the		
		difference in the rate at		
6		which two devices can		
Ĭ		handle data during a		
7		transfer; Dictionary of		
´		Computing (1st ed. 1983):		
8		A temporary memory for		
		data, normally used to		
9		accommodate the difference		
		in the rate at which two		
10		devices can handle data		
10		during a transfer. The		
11		buffer may be built into a		
11		peripheral device, such as a		
12		printer or disk drive, or may		
14		be part of the system's main		
13		memory; <u>IBM Dictionary of</u>		
13		Computing (10th ed. 1993): 1. A routine or storage used		
14		to compensate for a		
14		difference in rate of flow of		
15		data, or time of occurrence		
13		of events, when transferring		
16		data from one device to		
10		another. 4. A portion of		
17		storage used to hold input or		
1 /		output data temporarily;		
18		Microsoft Computer		
10		Dictionary (5th ed. 2002): A		
19		region of memory reserved		
1)		for use as an intermediate		
20		repository in which data is		
20		temporarily held while		
21		waiting to be transferred		
_1		between two locations or		
22		devices; Webster's New		
		World Computer Dictionary		
23		(10th ed. 2003): A unit of		
23		memory given the task of		
24		holding information temporarily, especially		
		while waiting for slower		
25		components to catch up.		
ادے		components to caten up.		
26		INTRINSIC EVIDENCE:		
الاس		Claims: see, e.g., claim 6;		
27		("the buffer memory		
41		comprises a buffer		
28	L	TTPTIOTO W CHIEF	I .	I .
40				

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
4		independent of the host	Crimence	Crimence
3		address space"); see also		
		claim 1; claim 2; claim 3;		
4		claim 4; claim 11; claim 14; claim 16; claim 18; claim		
5		20; claim 22; claim 24;		
3		claim 25; claim 30; claim		
6		32; claim 34; claim 38;		
		claim 39; claim 40; claim		
7		42; claim 43; claim 44; claim 46; claim 47; claim		
		48; claim 49; claim 50;		
8		claim 52; Specification:		
9		see, e.g., figs. 2, 6, 7, 9, 11-		
		13 col. 2:38-41 ("The		
10		apparatus includes network interface logic for		
		transferring the data frame		
11		between the network		
12		transceiver and a buffer		
14		memory for storing the data frame."); see also col. 1:25-		
13		36; col. 1:39-45; col. 2:1-5;		
		col. 2:41-43; col. 2:46-50;		
14		col. 2:55-3:7; col. 3:18-22;		
1		col. 3:44-46; col. 3:57-67;		
15		col. 4:38-48; col. 6:27-32; col. 6:34-38; col. 7:1-2; col.		
16		7:16-20; col. 7:61-63; col.		
		10:18-25; col. 10:30-32; col.		
17		10:37-40; col. 10:42-45; col.		
1.0		10:48-51; col. 10:58-61; col. 10:66-68; col. 11:23-26; col.		
18		11:29-36; col. 11:43-47; col.		
19		11:49-52; col. 12:34-37; col.		
17		12:47-49; col. 13:18-21; col.		
20		13:34-41; col. 13:43-49; col. 13:53-56; col. 13:58-68; col.		
		14:1-4; col. 14:6-21; col.		
21		14:26-29; col. 14:34-40; col.		
22		14:59-62; col. 15:67-16:8;		
22		col. 16:15-20; col. 16:34-37;		
23		col. 16:43-55; col. 16:61-62; col. 17:5-9; col. 17:41-47;		
		col. 17:52-53; col. 17:55-59;		
24		col. 17:61-62; col. 18:4-7;		
25		col. 18:23-27; col. 18:30-34;		
25		col. 18:47-51; col. 18:62-66; col. 19:2-17; col. 19:19-26;		
26		col. 19:28-32; col. 19:49-51;		
		col. 19:60-68; col. 20:16-22;		
27		col. 20:45-48; col. 20:55-58;		
28		col. 20:60-68; col. 21:1-3;		

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	col. 22:12-14; col. 23:60-64;		
	col. 24:12-15; col. 24:28-30;		
	col. 24:38-44; col. 24:56-59;		
	col. 24:63-68; col. 25:12-19;		
	col. 25:21-24; col. 25:35-41;		
	col. 25:62-63; col. 26:1-3;		
	col. 26:40-42; col. 26:65-67;		
	col. 27:53-55; col. 28:4-6;		
	col. 28:20-22; col. 33:26-33;		
	col. 34:25-28; col. 38:14-17;		
	see also Prosecution		
	History: Notice of		
	Allowability, Oct. 14, 1993,		
	pp. 2-3.		
	EXTRINSIC EVIDENCE:		
	See section I.A, supra		
	(agreed upon definition for		
	"buffer" in '625 and '884		
	patents). 3Com's expert,		
	Dr. Michael Mitzenmacher		
	may provide an expert		
	report or other form of		
	testimony regarding the		
	technology to which this		
	term relates and how a		
	person having ordinary skill		
	in the art in the field of		
	networking technology		
	would understand this term.		
	3Com reserves the right to		
	rely on testimony by any		
	expert in this action.		
	See also U.S. Patent Nos.		
	5,434,872; 5,732,094;		
	6,327,625; 6,526,446; and		
	6,570,884; Joint Claim		
	Construction Statement in		
	Cv-05-00098 (VRW).		
	3Com reserves the right to		
	rely on any statement made		
	by any party under the		
	Patent Local Rules.		
"buffer memory"	PROPOSED CONSTRUCTION:	Dronger congenuetion:	Droposer construction:
butter memory	A memory for temporary	PROPOSED CONSTRUCTION: Dedicated random access	PROPOSED CONSTRUCTION: A memory that (1) stores
found in claim	storage of data.		frame data such that the
numbers:	storage of data.	memory that (1) stores	frame data can be retrieved
numbers.	DICTIONARY/TREATISE	transmit data, (2) is distinct	independently of the order
'459 patent: 1	DEFINITIONS: See "buffer"	from a FIFO, (3) can always	in which the frame data
107 patent. 1	above; memory: Dictionary	retransmit a frame of data	were stored and the frame
-1 1 C	of Computing (1st ed.	without having to retrieve it	data can always be retained
also presented for	I OI COMBUME USEGO		

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
	construction in:	1983): A device or medium	from a host, and (4)	and reused and can be
3	(070 ) 1 10 01	that can retain information	controlled independently of	accessed by the host system;
_,	'872 patent: 1, 10, 21	for subsequent retrieval.	the host system.	and (2) is not a first-in-first-
4	'094 patent: 1, 9, 21,	The term is synonymous with storage and store,	L	out (FIFO) system.
5	28, 39, 47	although it is most frequently used for referring	INTRINSIC EVIDENCE:	INTRINSIC EVIDENCE:
6		to the internal storage of a	PATENT SPECIFICATION: "The transmit data buffer	'872 patent at 1:47-54; '094
7		computer that can be directly addressed by	occupies 3K bytes as mentioned above. This	patent at 1:44-50 ("Transmit data buffers are to be
Ó		operating instructions; see also The American Heritage	region is divided into two 1.5K buffers. Only the data	distinguished from first-in- first-out FIFO systems, in
8		Dictionary of the English Language (4th ed. 2000):	that are downloaded to the adapter via bus master	which the sending system downloads data of a frame
9		Computer Science. a. A unit of a computer that preserves	transfers are stored in these	into the FIFO, while the network adapter unloads the
10		data for retrieval. b. Capacity for storing	buffers. The controller will use both the contents of the	FIFO during a transmission.  The data in FIFOs cannot
11		information: two gigabytes	transmit data buffer and the immediate data portion of	be retained and reused by
12		of memory.	the transmit descriptors, when encapsulating a frame	the media access control functions, or by the host,
13		<u>Intrinsic evidence</u> : <u>Claims</u> : <u>see, e.g.</u> , claim 6;	for transmission. The adapter automatically	like data in transmit data buffers.")
14		("the buffer memory comprises a buffer	alternates the use of the buffers after choosing the	'872 patent at 1:65-2:2; '094
15		independent of the host address space"); see also	buffer closest to the base of the memory as the power up	patent at 1:60-65 ("Furthermore, the prior art
16		claim 1; claim 2; claim 3; claim 4; claim 11; claim 14;	default." ('459; Col. 13: 59-	systems which use transmit data buffers require the host
		claim 16; claim 18; claim 20; claim 22; claim 24;	68) (emphasis added).	or sending system to manage the transmit data
17		claim 25; claim 30; claim	"Some network adapter interfaces include dedicated	buffer. A network interface controller transfers data
18		32; claim 34; claim 38; claim 39; claim 40; claim	transmit buffers into which a frame of data composed	from the host managed
19		42; claim 43; claim 44; claim 46; claim 47; claim	by the sending system can be downloaded by the	transmit data buffer using DMA techniques through a
20		48; claim 49; claim 50; claim 52; Specification: see,	sending system. The frame is then stored in the <i>transmit</i>	FIFO buffer in the interface controller and on to the
21		e.g., figs. 7-9; col. 2:38-41 ("The apparatus includes	data buffer until the media	network.")
22		network interface logic for transferring the data frame	access control functions associated with transmitting	'872 patent at 2:7-10; '094 patent at 2:3-5 ("It is
23		between the network transceiver and a buffer	the frame on the network have successfully	desirable to provide the advantages of a transmit
24		memory for storing the data frame."); see also col. 1:25-	transmitted the frame, or cancelled the frame	data buffer, while maintaining the
25		36; col. 1:39-45; col. 2:1-5;	transmission. If the frame	communications throughput
		col. 2:41; col. 2:46-50; col. 2:55-3:7; col. 3:18-22; col.	transmission is cancelled, the data may be retained in	available from the simpler FIFO based systems.")
26		3:44-46; col. 3:57-67; col.	the transmit data buffer	2272 notant at 2:25 55: 2004
27		7:16-19; col. 34:25-28; see also Prosecution History:	until the sending system initiates a second attempt to	'872 patent at 2:35-55; '094 patent at 2:28-52
		Notice of Allowability, Oct.	transmit the frame.	("According to another
28				

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	14, 1993, pp. 2-3.	Transmit data buffers are to	aspect of the present invention, the transmit
	EXTRINSIC EVIDENCE:	be distinguished from first-	buffer includes a transmit
	See section I.A, supra	in-first-out FIFO systems, in which the sending system	descriptor ring, and a
	(agreed upon definition for	downloads data of a frame	transmit data buffer
	"buffer" in '625 and '884	into the FIFO, while the	
	patents); 3Com's expert, Dr.	network adapter unloads the	'872 patent at 13:17-48;
	Michael Mitzenmacher may	FIFO during a transmission.	'094 patent at 12:44-13:5
	provide an expert report or	The data in FIFOs cannot be	("A. Transmit Data Buffer
	other form of testimony	retained and reused by the	
	regarding the technology to	media access control	The transmit data buffer
	which this term relates and	functions, or by the host,	occupies 3K bytes as
	how a person having	like data in <i>transmit data</i>	mentioned above. This
	ordinary skill in the art in the field of networking	buffers." ('872; Col. 1: 36-	region is divided into two 1.5K buffers. Only the data
	technology would	54) (emphasis added).	that are downloaded to the
	understand this term. 3Com		adapter via bus master
	reserves the right to rely on	PROSECUTION HISTORY:	transfers are stored in these
	testimony by any expert in	m 0.11 · · ·	buffers. The controller wil
	this action.	The following citation to	use both the contents of the
		the prosecution history of	transmit data buffer and th
	See also U.S. Patent Nos.	the '872 patent supports D- Link's proposed claim	immediate data portion of
	5,434,872; 5,732,094;	construction.	the transmit descriptors,
	6,327,625; 6,526,446; and 6,570,884; Joint Claim	construction.	when encapsulating a fram for transmission
	Construction Statement in	During prosecution of the	The transmit buffers are
	Cv-05-00098 (VRW).	application that issued as the	shared by the download
	(1111).	'872 patent, in a Response	DMA logic and the transm
	3Com reserves the right to	dated February 23, 1994,	DMA logic. The transmit
	rely on any statement made	3Com stated the following:	DMA logic may switch
	by any party under the	// 1: 1 · 1	from buffer 0 to buffer 1
	Patent Local Rules.	"Accordingly, the	and back again freely. The
		Firoozmand, et al. reference does not initiate	only restriction being the
		transmission to the network	availability of transmit dat
		upon the threshold	as defined by the transmit start threshold register
		determination. Rather,	.")
		transmission to the network	· <i>)</i>
		is initiated only when there	'872 patent, at 1:5-14
		is a full frame available in	("CROSS-REFERENCE
		the buffer. When the token	TO RELATED
		has been received by the	APPLICATIONS
		transmitting station, and it has a full frame for	The present application is
		transmission, then a	related to copending U.S.
		transmission process is	patent application entitled NETWORK INTERFACE
		begun. The transmission	WITH HOST
		process continues, relying	INDEPENDENT BUFFER
		on the threshold	MANAGEMENT,
		determination to keep the	application Ser. No.
		pipeline full, only while the	07/921,519, filed 28 Jul.
		token is held by the	1992, now U.S. Pat. No.
	1	1	5,299,313, which was

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		transmitting station."	owned at the time of
			invention and is currently
		"The environment is	owned by the same
		substantially different from	assignee.")
		the CSMA/CD network,	450 potent at 1:5 12
		which begins transmission to the medium access	'459 patent, at 1:5-13 ("CROSS-REFERENCE
		controller as soon as the	TO RELATED
		threshold determination is	APPLICATIONS
		met for an incoming frame.	The present application is
		The MAC may succeed in	related to copending U.S.
		transmitting the frame, may	patent application entitled
		suffer collisions, or may	NETWORK INTERFACE
		suffer other types of errors	WITH HOST
		which require backoff.	INDEPENDENT BUFFER
		Thus, the adapter as claimed	MANAGEMENT, Ser. No.
		in new claims 24-29,	07/921,519, filed Jul. 28,
		initiates transmission	1992, which was owned at
		without being assured that	the time of invention and is
		the medium access	currently owned by the
		controller is able to gain	same assignee.")
		access to the	4450
		communications medium.	'459 patent, at 13:58-14:22
		This is a much more	("A. Transmit Data Buffer
		sophisticated control environment than that	The transmit data buffer
		required by the FDDI	occupies 3K bytes as
		system of Firoozmand, et	mentioned above. This
		al."	region is divided into two
			1.5K buffers. Only the data
		Response dated February	that are downloaded to the
		23, 1994, p. 5.	adapter via bus master
			transfers are stored in these
		EXTRINSIC EVIDENCE:	buffers. The controller will
			use both the contents of the
		PRIOR ART:	transmit data buffer and the
			immediate data portion of
		Datesheet for "82596CA	the transmit descriptors,
		High-Performance 32-Bit	when encapsulating a frame for transmission The
		Local Area Network	transmit buffers are shared
		Coprocessor," November	by the download DMA log
		1989, Intel Corp (Disclosed in D-Link's Preliminary	and the transmit DMA
		Infringement Contentions),	logic. The transmit DMA
		pg. 2: "Two large,	logic may switch from
		independent FIFOs-128	buffer 0 to buffer 1 and bac
		bytes for Receive and 64	again freely. The only
		bytes for Transmit-tolerate	restriction being the
		long bus latencies and	availability of transmit data
		provide programmable	as defined by the transmit
		thresholds that allow the	start threshold register. The
		user to optimize bus	transmit DMA module
	1	overhead for any worst-case	switches from one buffer to

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	the other whenever it has
		bus latency."	completed a transmission.
			The buffer switch occurs
		Datasheet for "The	regardless of whether or n
		SUPERNET 2 Family for	the transmission was
		FDDI", October 1991,	successful and regardless
		Advanced Micro Devices,	whether or not bus master
		Inc. (Disclosed in D-Link's	download data were used
		Preliminary Infringement	the preceding transmission
		Contentions), pg. 2-37: "The transmit FIFO (Figure	")
		1) is a 36-bit by 9-word	DICTIONARY/TREATISE
		first-in-first-out register that	DEFINITIONS:
		temporarily stores data to be	
		transmitted. In this way,	The Network Interface
		continuity of data	Technical Guide, (First
		transmission is assured by	Edition, 1992)
		providing a way to store a	Buffer: A temporary stora area in random access
		portion of the output data stream to compensate for	memory where the NIC or
		delays involved in accessing	computer stores informati
		the buffer memory."	(usually while transmittin
			or receiving network
		1992 Local Area Network	traffic).
		<u>Databook Including</u>	
		Datasheet For DP83932B	EXPERT TESTIMONY:
		Systems-Oriented Network	Dooltoly's over out Dr. Inho
		Interface Controller (SONIC), 1992, National	Realtek's expert, Dr. Izha Rubin, may provide
		Semiconductor Corp, pg.1-	testimony as to the
		295: "The SONIC	definition of the disputed
		incorporates two	terms as would be
		independent 32-byte FIFOs	understood by one of
		for transferring data to/from	ordinary skill in the releva
		the system interface and	art and may provide an
		from/to the network. The	explanation of the technology.
		FIFOs, providing temporary storage of data, free the host	technology.
		system from the real-time	PRIOR ART:
		demands on the network."	
			Datesheet for "82596CA
		DICTIONARY/TREATISE	High-Performance 32-Bit
		DEFINITIONS:	Local Area Network
		McCroyy Hill Hlychecks d	Coprocessor," November
		McGraw-Hill Illustrated Telecom Dictionary, Fourth	1989, Intel Corp, pg. 2 ("Two large, independent
		Edition, 2001, pg. 83:	FIFOs-128 bytes for
		Buffer - "A temporary	Receive and 64 bytes for
		storage (memory) device for	Transmit-tolerate long bus
		data. A buffer is basically a	latencies and provide
		box with RAM inside it. A	programmable thresholds
		common application for	that allow the user to
		buffers is to collect a stream	optimize bus overhead for

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
	evidence	of data and temporarily	any worst-case bus
		store it until another device,	latency.")
		such as a PC or server asks	
		the buffer to download it.	Datasheet for "The
		This is useful when the PC,	SUPERNET 2 Family for
		server or LAN could be out	FDDI", October 1991,
		of service for a period of	Advanced Micro Devices,
		time. When the server or PC is returned to service it	Inc., pg. 2-37
		just asks for the data from	("The transmit FIFO (Figur 1) is a 36-bit by 9-word
		the buffer and it is	first-in-first-out register tha
		downloaded. The buffer is	temporarily stores data to be
		then empty and ready to	transmitted. In this way,
		receive more data."	continuity of data
			transmission is assured by
		EXPERT TESTIMONY:	providing a way to store a
			portion of the output data
		D-Link's expert, Howard	stream to compensate for
		Frazier, may provide	delays involved in accessing
		testimony as to the	the buffer memory.")
		definition of the disputed terms as would be	1992 Local Area Network
		understood by one of	Databook Including
		ordinary skill in the relevant	Datasheet For DP83932B
		art and may provide an	Systems-Oriented Network
		explanation of the	Interface Controller
		technology.	(SONIC), 1992, National
			Semiconductor Corp, pg.1-
		D-Link also incorporates by	295:
		reference Realtek's cited	("The SONIC incorporates
		references.	two independent 32-byte
			FIFOs for transferring data to/from the system interface
			and from/to the network.
			The FIFOs, providing
			temporary storage of data,
			free the host system from
			the real-time demands on
			the network.")
			Ethernet/IEEE-802.3 Family
			1990 World Network Data
			Book/Handbook, Advanced Micro Devices, pg. 1-63,
			("FIFO Operations
			( I II O Operations
			The FIFO provides
			temporary buffer storage fo
			data being transferred
			between the parallel bus I/O
			pins and serial bus I/O pins
			The capacity of the FIFO is
	1	Ī	48 bytes.

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
(disputed terms in both)	evidence	evidence	evidence
			Transmit
			Data is loaded into the FIFO under internal micro-
			program control. The FIFO must be more than 16 bytes empty before
			the ILACC requests the bus (HOLD/BURREQ is
			asserted). The ILACC will start sending the preamble
			(if the line is idle) as soon a there is one byte loaded int the FIFO. Should the
			transmitter be required to back off, there will be up to
			32 bytes of data in the FIFO ready for transmission.
			Reception has priority over transmission during the time that the transmitter is
			backing off.
			Receive
			Data is loaded into the FIF from the serial input shift
			register during reception and leaves the FIFO under microprogram control. The
			ILACC microcode will wa until there are at least 16
			bytes of data in the FIFO before initiating a DMA burst transfer. Preamble
			(including the synchronization bits) is not loaded into the FIFO.")
"host system"	PROPOSED CONSTRUCTION: A computer that	PROPOSED CONSTRUCTION: Any system or computer	PROPOSED CONSTRUCTION: Any system or computer
found in claim numbers:	communicates over a network	that communicates over a network	that communicates over a network
'459 patent: 1	<u>DICTIONARY/TREATISE</u> <u>DEFINITIONS:</u> Webster's New	INTRINSIC EVIDENCE	Evidence
also presented for construction in:	World Computer Dictionary (10th ed. 2003): 1. In the	(872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62)	(872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62)
'872 patent: 1, 10, 21	Internet, any computer that can function as the	Furthermore, the prior art systems which use transmit	Furthermore, the prior art systems which use transmir
072 patent. 1, 10, 21	beginning and end point of	data buffers require the <i>host</i>	data buffers require the hos

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
1	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2	(displica terms in both)	evidence	evidence	evidence
~		host has a unique Internet	manage the transmit data	manage the transmit data
3	'884 patent: 1	address (called an IP	buffer.	buffer.
	P	address) and a unique	ourier.	ourier.
4		domain name. 2. In	(872: Col. 3, ln. 65 to col.	(872: Col. 3, ln. 65 to col.
1		networks and	4., ln. 2) ('094: Col. 3, lns.	4., ln. 2) ('094: Col. 3, lns.
5		telecommunications	59-64) As shown in FIG. 1,	59-64) As shown in FIG. 1,
		generally, a server that	such system for	such system for
6		performs centralized	communicating data	communicating data
		functions, such as making	includes a host data	includes a host data
7		program or data files	processing system,	processing system,
		available to other	generally referred to by	generally referred to by
8		computers; The American	reference number 1, which	reference number 1, which
		Heritage Dictionary of the	includes a host system bus	includes a host system bus
9		English Language (4th ed.	2, a host central processing	2, a host central processing
		2000): Computer Science. A	unit 3, host memory 4, and	unit 3, host memory 4, and
10		computer containing data or	other host devices 5, all	other host devices 5, all
		programs that another	communicating across the	communicating across the
11		computer can access by	bus 2	bus 2
		means of a network or		
12		modem; <u>Dictionary of</u>		(004 0 4 0 4 0 4 0
12		Computing (3d ed. 1990):		(884: Col. 2, lns. 39-44)
13		Host computer (host): A		The invention is particularly
14		computer that is attached to		suited to environments in
14		a network and provides		which the host system is
15		services other than simply		actively handling communications and other
		acting as a store-and- forward processor or		processing tasks, and in
16		communication switch.		which the adapter is able to
		Communication switch.		take over some specialized
17		INTRINSIC EVIDENCE:		tasks without interfering
- /		Claims: claim 1; claim 3;		with the active processing in
18		claim 4; claim 5; claim 6;		the host system.
		claim 11; claim 16; claim		
19		18; claim 22; claim 23;		
		claim 24; claim 25; claim		
20		30; claim 34; claim 35;		
		claim 38; claim 39; claim 40; claim 41; claim 42;		
21		claim 44; claim 45; claim		
		46; claim 47; claim 48;		
22		claim 50; claim 51; claim		
22		52; claim 53; Specification:		
23		see, e.g., col. col. 5:66-68		
24		("The host system further		
<b>4</b>		includes host memory 6,		
25		host processor 5, and other		
د ـ		host devices 7 coupled to		
26		host bus 4.)"; see also col. 1:20-23; col. 1:23-25; col.		
		1:20-23; col. 1:23-25; col. 1:25-31; col. 1:31-37; col.		
27		1:37-38; col. 1:38-42; col.		
- '	L	1.57 50, 601. 1.50 42, 601.		1

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	1:42-46; col. 1:46-51; col.		
	1:51-54; col. 1:54-56; col.		
	1:56-59; col. 1:59-63; col.		
	1:63-66; col. 1-2:66-1; col.		
	2:1-6; col. 2:6-8; col. 2:8- 13; col. 2:18-22; col. 2:22-		
	28; col. 2:30-32; col. 2:32-		
	35; col. 2:35-37; col. 2:37-		
	38; col. 2:41-43; col. 2:43-		
	46; col. 2:52-55; col. 2:55-		
	59; col. 2:59-63; col. 2:63-		
	67; col. 2-3:67-2; col. 3:8-		
	11; col. 3:11-15; col. 3:25-		
	28; col. 3:28-33; col. 3:44-		
	47; col. 3:61-65; col. 3:65-		
	67; col. 4:21-24; col. 4:28-		
	31; col. 4:31-34; col. 4:34-		
	36; col. 4:45-49; col. 5:56-		
	58; col. 5:58-60; col. 5:61-		
	62; col. 5:62-64; col. 5:64-		
	66; col. 5:66-68; col. 6:2-5;		
	col. 6:5-9; col. 6:15-19; col.		
	6:19-23; col. 6:29-32; col.		
	6:34-38; col. 6:38-41; col.		
	6:41-44; col. 6:44-48; col.		
	6:48-53; col. 6:53-60; col.		
	6:61-63; col. 7:9-12; col.		
	7:16-19; col. 7:21-23; col.		
	7:54-56; col. 7:61-63; col.		
	8:8-11; col. 8:46; col. 9:20-		
	24; col. 9:24-27; col. 9:34-		
	36; col. 9:38-43; col. 9:57-		
	59; col. 10:5-8; col. 10:16-		
	18; col. 10:25-30; col.		
	11:29-33; col. 11:36-40; col.		
	11:43-45; col. 11:52-56; col.		
	11:56-60; col. 11:60-64; col.		
	11:64-66; col. 12:4-7; col. 12:18-22; col. 12:22-24; col.		
	12:24-58; col. 12:58-29; col.		
	12:29-30; col. 12:30-33; col.		
	12:39-43; col. 12:43-47; col.		
	12:47-50; col. 12:58-60; col.		
	12:60-66; col. 12:66-67; col.		
	12-13:67-3; col. 13:8-12;		
	col. 13:12-14; col. 13:14-16;		
	col. 13:16-18; col. 13:25-26;		
	col. 13:34-37; col. 13:37-42;		
	col. 13:42-43; col. 14:32-34;		
	col. 14:41-46; col. 14:46-48;		
	col. 15:4-7; col. 15:10-12;		
	col. 15:23-27; col. 15:30-32;		
	col. 15:36-39; col. 15:39-42;		

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	col. 15:42-45; col. 15:52-55;		
	col. 15:61-62; col. 15:62-67;		
	col. 15:67-1; col. 16:1-3;		
	col. 16:3-6; col. 16:9-13;		
	col. 16:13-15; col. 16:16-19;		
	col. 16:22-24; col. 16:34-37;		
	col. 16:37-40; col. 16:43-45;		
	col. 16:47-48; col. 17:1-4;		
	col. 17:12-15; col. 17:33-35;		
	col. 17:45-47; col. 17:52-53;		
	col. 17:55-58; col. 18:4-7;		
	col. 18:7-9; col. 18:9-17;		
	col. 18:19-22; col. 18:24-27;		
	col. 18:27-29; col. 18:30-35;		
	col. 18:47-51; col. 18:51-53;		
	col. 18:53-56; col. 18:56-58;		
	col. 18:58-62; col. 18:62-66;		
	col. 19:9-14; col. 19:29-34;		
	col. 19:34-36; col. 19:36-42;		
	col. 19:46-47; col. 19:47-49;		
	col. 19:52-55; col. 19:64-66;		
	col. 20:1-5; col. 20:13-16;		
	col. 20:16-24; col. 20:37-40;		
	col. 20:43-45; col. 20:49-53;		
	col. 21:4-8; col. 21:9-11;		
	col. 21:11-16; col. 21:16-18;		
	col. 21:22-25; col. 21:40-42;		
	col. 22:18-23; col. 22:49-52;		
	col. 23:6-9; col. 23:30-33;		
	col. 23:37-39; col. 23:43-47;		
	col. 23:60-64; col. 24:17-19;		
	col. 24:19-22; col. 24:31-34;		
	col. 24:34-37; col. 24:38-40;		
	col. 24:48-51; col. 24:51-52;		
	col. 24:63-1; col. 25:1-2;		
	col. 25:2-6; col. 25:6-7; col.		
	25:28-31; col. 25:31-33; col.		
	25:53-55; col. 25:55-56; col.		
	25:56-57; col. 25:57-60; col.		
	25:62-65; col. 25:65-1; col.		
	26:18-21; col. 26:22-23; col.		
	26:25-26; col. 26:27-29; col.		
	26:29-32; col. 26:32-35; col.		
	26:37-39; col. 26:40-43; col.		
	27:16-17; col. 27:22-26; col.		
	27:45-47; col. 27:47-52; col.		
	27:52-55; col. 27:55-60; col.		
	28:7-9; col. 28:11-13; col.		
	28:17-20; col. 28:22-24; col.		
	28:24-26; col. 28:27-30; col.		
	28:31-33; col. 28:42-46; col.		
	29:9-12; col. 29:12-15; col.		
	29:23-25; col. 30:10-13; col.		

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	30:44-47; col. 30:47-48; col.		
	30:48-51; col. 30:51-55; col.		
	30:55-57; col. 30:64-67; col.		
	32:13-15; col. 32:39-44; col.		
	32:62-65; col. 32:65-68; col.		
	33:9-12; col. 33:12-15; col.		
	33:28-33; col. 33:33-40; col.		
	33:40-46; col. 33:46-49; col.		
	34:20-22; col. 34:25-28; col.		
	34:28-31; col. 34:38-41; col.		
	34:43-46; col. 34:46-50; col.		
	34:50-52; col. 35:36-38; col.		
	35:38-41; col. 35:44-46; col.		
	35:51-53; col. 36:40-42; col.		
	36:44-46; col. 38:12-14; col.		
	39:31-38; col. 39-40:67-3; col. 41:34-40; col. 41:44-46;		
	col. 41:46-51; col. 42:6-11;		
	col. 42:17-19; col. 42:19-22;		
	col. 42:22-25; see also		
	Prosecution History: Notice		
	of Allowability, Oct. 14,		
	1993, pp. 2-3.		
	1995, pp. 2 5.		
	EXTRINSIC EVIDENCE:		
	3Com's expert, Dr. Michael		
	Mitzenmacher may provide		
	an expert report or other		
	form of testimony regarding		
	the technology to which this		
	term relates and how a		
	person having ordinary skill		
	in the art in the field of		
	networking technology		
	would understand this term.		
	3Com reserves the right to		
	rely on testimony by any		
	expert in this action.		
	Caralas II C. Dataut Nas		
	See also U.S. Patent Nos. 5,434,872; 5,732,094;		
	6,327,625; 6,526,446; and		
	6,570,884; Joint Claim		
	Construction Statement in		
	Cv-05-00098 (VRW).		
	CV-03-00078 (VKW).		
	3Com reserves the right to		
	rely on any statement made		
	by any party under the		
	Patent Local Rules.		
"indication signal"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
	A signal that indicates a	A signal that indicates the	A signal that is not an
found in claim	subsequent action, such as	timing for a subsequent	interrupt but may be used b
		<u> </u>	

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disputed terms in bold)  construction and supporting evidence widence an interrupt  an interrupt  an interrupt  birthomary/TREATISE DEFINITIONS: indication: The American Heritage Dictionary of the English Language (4th ed. 2000); Something that serves to indicate; a sign, signal: The American Heritage Dictionary of the English Language (4th ed. 2000); An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics An impulse or a fluctuating electric quantity, such as a voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983). Indicator: A bit or bit configuration that may be inspected to determine a status or condition. Bim Dictionary of Computing (10th ed. 1993): Indicator: A doit or bit configuration that may be inspected to determine a status or condition. Bim Dictionary of Computing (3d ed. 1990): Indicator: A doit or bit configuration that may be inspected to determine a status or condition. Bim Dictionary of Computing (3d ed. 1990): Indicator: A doit or bit configuration that may be inspected to determine a status or condition. Electroic of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A doit or bit configuration that may be inspected to determine a status or condition; lamb Dictionary of Computing (3d ed. 1990): Indicator: A doit or bit configuration that may be inspected to determine a status or condition; lamb Dictionary of Computing (3d ed. 1990): Indicator: A doit or bit configuration that may be inspected to determine a status or condition; lamb Dictionary of Computing (3d ed. 1990): Indicator: A doit or bit configuration that may be inspected to determine a status or condition; lamb Dictionary of Computing (3d ed. 1990): Indicator is doited to the condition signal includes an early receive signal?); see also claim 1; claim 5; claim 3; claim 17; claim	1 Claim language	2Com's proposed	D-Link's proposed	Dogletak's proposed
numbers: an interrupt  A 59 patent: 1  DICTIONARY/TREATISE  DETENTIONS: indication: The American Heritage Dictionary of the English Language (4th ed. 2000): Something that serves to indicate; a sign; signal: The American Heritage Dictionary of the English Language (4th ed. 2000): An indicator; such as a gesture or colored light, thas erves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as a voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  Dictionary of Computing (3d ed. 1990): Indicator: A divide that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  NETRINSIC EVIDENCE: Claims; see, e.g., claim 12, claim 17, claim 19, claim 19, claim 27, claim 27, claim 22, claim 32, claim 31; claim 17, claim 19, claim 21, claim 21, claim 22, claim 32, claim 31; claim 17, claim 19, claim 21, claim 21		3Com's proposed		Realtek's proposed
3 '459 patent: 1  DICTIONARY/TREATISE DEFENITIONS: indication: The American Hertiage Dictionary of the English Language (4th ed. 2000): Something that serves to indicate; a sign; signal: The American Hertiage Dictionary of the English Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics: An impulse or a fluctuating electric quantity, such as a yoltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio television, or radar; see also Dictionary of Computing (15t ed. 1983) Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  10 determine a status or condition.  11 Image, or message transmitted or received in telegraphy, telephony, radio television, or radar; see also Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication signal and by the substitution of a data frame is completed." ('459) patent at 1:20-2 state of a defined state; Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication signal and a host computer system; the transfer of data frame is completed." ('459) Abstract).  10	2	evidence	evidence	evidence
Variations represent coded information. The Sound, image, or message transmitted or received in telegraphy, telephony, radio, inage, or radar; see also plictionary of Computing (10th ed. 1993). Indicator: A device that gives a visual or condition. The Abit or bit configuration that may be inspected to determine a status or condition. The status or condition. The status or condition. The status or condition. The column and the host system. The firm is completed." (*459) patent, Abstract (*500) primized indication signals of a completed data frame transfer are generated by a network adapter which reduces host processor interrupt. The network adapter which reduces the transferring the data frame between the network and a valure framemory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host interface logic for transferring		an interrupt	action, such as an interrupt	the host system to generate an interrupt.
The American Heritage Dictionary of the English Language (4th ed. 2000): Something that serves to indicate; a sign, signal: The American Heritage Dictionary of the English Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983): Indicator: A device that gives a visual or other indication of the existence of a definied state; Dictionary of Computing (19th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a definied state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition, 1990): Indicator: A device that gives a visual or other indication of the existence of a definied state; Dictionary of Computing (3d ed. 1990): Indicator: A device that gives a visual or other indication of the existence of a definied state; Dictionary of Computing (3d ed. 1990): Indicator: A device that gives a visual or other indication signal to a host processor of the completed transfer of at targenerate an early indication signal may be used to generate an early indication or a data frame transfer or a data f	'459 patent: 1		REFERENCES:	-
Dictionary of the English   Language (4th ed. 2000): Something that serves to indicate; a sign; signal: The American Heritage   Dictionary of the English   Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuation   Heritage   Dictionary of the English   Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuation   Electronics. An impulse or a fluctuation   Electronics. An impulse or a fluctuation   Electronics   Ele	4		PATENT SPECIFICATION:	INTRINSIC EVIDENCE:
Something that serves to indicate; a sign. signal: The American Heritage Dictionary of the English    Reserves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1993): Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition. IBM Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition. (1st ed. 1993): Indicator: A bit or bit configuration that may be inspected to determine a status or condition. (1st ed. 1993): Indicator: A bit or bit configuration that may be inspected to determine a status or condition. (1st ed. 1993): Indicator: A bit or bit configuration that may be inspected to determine a status or condition. (1st ed. 1993): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  NRTRINISIC EVIDENCE: Claims: see, e.g., claim 12 ("The indication signal includes an early receives signal"); see also claim 1; claim 5; claim 13; claim 17; claim 23; claim 23; claim 23; claim 23; claim 23; claim 23; claim 24; claim 25; claim 23; claim 25; claim 26; claim 26; claim 26; claim 26; claim 26; claim 26; claim 27; claim 27; claim 27; claim 28; claim 28; claim 28; claim 28; claim 28; claim 29; claim 29; claim 29; claim 20; claim 20	5	Dictionary of the English		'459 patent, Abstract
indicate; a sign.; signal: The American Heritage Dictionary of the English Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983). Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1993): Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC FUIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 23; claim 31; claim 17; claim 23; claim 31; claim 17; claim 23; claim 31; claim 17; claim 31; claim 13; claim 13; claim 17; claim 31; claim 13; claim 17; claim 31; claim 17; claim 31; claim 17; claim 31; claim 18; claim 13; claim 17; claim 31; claim 19; claim 31; claim 17; claim 31; claim 19; claim 31; claim 17; claim 31; claim 19; claim 31; claim 17; claim 31; claim 18; claim 18; claim 19; claim 31; claim 19; claim 31; claim 51; claim 18; claim 19; claim 31; claim 19; claim 31; claim 51; claim 19; claim 31; claim 19; claim 31; claim 19; claim 31; claim 19; claim 31; claim 31				` 1
Dictionary of the English Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition,  INTENSIC EVIDENCE: Claims; see, e.g., claim 12 ("the indication signal includes an early receive and a host computer system typically notify the host processor must take some action based on a completed transfer of a data frame between the buffer memory and host interface logic for transferring the data frame between the buffer memory and host further includes thre logic where a threshot further includes thre logic where a threshot further includes for transferring the data frame between the buffer memory and the host system. The network adapter swinder and a buffer memory and host includes threshold logic where a threshold logic where a threshold value in network adapter swinder further includes threa further includes th	6	_		
Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.    National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.   National Computing (3d ed. 1990): Indicator: A bit	7			generated by a network
An indicator, such as a gesture or colored light, thas serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983).Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTERNISIC EVIDENCE: Claims; see, e.g., claim 12; claim 13; claim 17; claim 19; claim 21; claim 31; clai	0			processor interrupt latency.
serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  18  19  10  11  12  13  14  15  15  16  16  17  16  17  18  17  18  19  18  19  19  10  10  10  11  10  11  11  11	8	An indicator, such as a	network adapter comprises	The network adapter
communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  18  19  20  20  21  21  22  23  24  25  24  25  26  27  28  28  29  29  20  20  21  21  22  23  24  25  26  26  27  28  28  29  29  20  20  21  21  22  23  24  25  26  26  27  27  28  28  29  29  20  20  20  20  21  21  22  23  24  25  26  26  27  28  29  29  20  20  20  21  21  22  23  24  25  26  26  27  28  29  29  20  20  20  20  21  21  22  23  24  25  26  26  27  28  29  29  20  20  20  20  21  21  22  23  24  25  26  26  27  28  29  29  20  20  20  20  20  21  21  22  23  24  25  26  26  27  27  28  28  29  29  29  20  20  20  20  20  20  20	9			
electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims; see, e.g., claim 12, claim 5; claim 13; claim 17; claim 19; claim 22, claim 23; claim 31;	10	communication. Electronics.	between the network and a	value in an alterable storage
voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983). Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  18  19  10  11  11  12  12  13  14  15  15  16  17  18  16  17  18  18  19  17  18  19  10  10  10  11  10  11  11  11  12  12	10	1		location is compared to a
variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983).Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  17  18  19  20  21  21  21  22  23  24  25  Intrinsic Evidence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  18  Intrinsic Evidence: Claims; see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 21; claim 22; claim 23; claim 31;  variations represent coded information. The sound, image, or message transmited or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983).Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  19  20  21  22  23  24  25  26  27  28  29  29  29  20  20  20  20  21  21  22  23  24  25  26  26  27  28  28  29  29  29  20  20  20  21  22  23  24  25  26  26  27  28  29  29  29  20  20  20  20  21  22  23  24  25  26  26  27  28  29  29  29  20  20  20  20  21  22  23  24  25  26  27  28  29  29  29  20  20  20  20  20  21  21  22  23  24  25  26  27  28  29  29  29  20  20  20  20  20  21  21  22  23  24  25  26  27  28  29  29  29  20  20  20  20  21  21  22  22  23  24  25  26  27  28  29  29  29  20  20  20  20  21  21  22  22  23  24  25  26  27  28  29  29  20  20  20  20  20  21  21  22  22  23  24  25  26  27  28  29  29  20  20  20  20  20  20  21  21  22  22	11	voltage, current, or electric	transferring the data frame	order to generate an early
information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983).Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993). Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990). Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1990). Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  18  19  20  20  21  22  23  24  25  26  27  28  Intrinsic Evidence: Claims; see, e.g., claim 12; claim 5; claim 13; claim 17; claim 19; claim 12; claim 22; claim 23; claim 31; claim 31; claim 31;	12		1	indication signal. The early
transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  The carly indication of the carly indication signal to a host processor before a transfer or data frame is completed")  The carly indication of the carly indication signal to a host processor before a transfer or data frame is completed")  The carly indication of the carly indication signal to a host processor before a transfer or data frame is completed")  The carly indication of the carly indication signal to a host processor before a transfer counter in order to generate an early indication signal transfer of a data frame is completed")  The carly indication of the carly indication signal to a host processor before a transfer counter in order to generate an early indication signal in the transfer of a data frame is completed")  The carly indication of the carly indication signal in the transfer of a data frame is completed")  The carly indication of the carly indication signal in the host processor of the transfer of a data frame is completed")  The carly indication of the carly indication signal transfer of a data frame is completed")  The carly indication of the carly indication signal transfer of a data frame is completed"  The carly indication of the carly indication signal in the host processor of the composition of the existence of a data frame transfer of the composition of the composition of the existence of a data frame transfer of a data frame transfer. In many circums				used to generate an early
telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 12; claim 22; claim 23; claim 31;	13			interrupt signal to a host
Dictionary of Computing (1st ed. 1983).Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993). Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990). Indicator: A bit or bit configuration that may be inspected to determine a status or condition.    19	14			
(1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.    20	1.5			completed ")
bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 19; claim 21; claim 22; claim 23; claim 31;  bit or bit configuration that may be inspected to determine a status or condition.  Signal. The early indication signal may be used to generate an early interrupt signal to a host processor in the transfer of a data frame is completed." ("459, Abstract).  Network adapters in volved in the transfer of data frame is completed." ("459, Abstract).  "Network adapters involved in the transfer of data frame setween a communications network and a host computer system typically notify the host processor of the component of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame transfer of the completed transfer of the completed transfer of a data frame. For example, if the network adapter has received a data frame in the network adapter has received a data frame, the host processor may need to	15			'459 patent at 1:20-2:27("2.
determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Obit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal to a host processor before a transfer of a data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Network adapters in in the transfer of data frame is completed." ("459, Abstract).  Not a data frame transfer. In many circumstances, the host processor of the completion of a data frame transfer of a data frame transfer. In many circumstances, the host processor must as some action based on a communications network and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must are communications network and a host computer system typically notify the host processor of the completion of a	16		signal. The early indication	Description of Related Art
condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Obictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 22; claim 23; claim 21; claim 22; claim 23; claim 21; claim 22; claim 23; claim 31;  signal to a host processor before a transfer of a data frame is completed." ("459, Abstract).  "Network adapters involved in the transfer of data frame is completed." ("459, Abstract).  "Network adapters involved in the transfer of data frame between a communications net work and a host computer typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a communications net work and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a communications net work and a host computer system typically notify the host processor of the completion of a data frame transfer of adata frame transfer. In many circumstances, the host processor must take some action based on a communications net volved in the transfer of data frame is completed." ("459, Abstract).  "Network adapters involved in the transfer of data frame is completed." ("459, Abstract).  "Network adapters involved in the transfer of data frame setween a communications net volved and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a communications network and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor may received a data fra	17			Network adapters involved
1993): Indicator: A device that gives a visual or other indication of the existence of a defined state;  20	1 /		signal to a host processor	in the transfer of data
that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  21  22  23  24  25  26  190  190  20  21  22  23  24  25  26  26  27  28  29  20  20  20  20  20  20  21  20  21  22  23  24  25  26  26  27  28  29  29  20  20  20  20  20  20  20  20	18			frames between a communications network
of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 22; claim 23; claim 31;  "Network adapters involved in the transfer of data frames between a communications network and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame in the network adapter has received a data frame, the host processor may need to other host devices on other host devices or of the computation of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to of a data frame transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to other host devices of the computation of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to	19	that gives a visual or other	1	and a host computer system
Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 19; claim 19; claim 22; claim 23; claim 31;  Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or communications network and a host computer system typically notify the host processor of the completion of a data frame trans many circumstances host processor must some action based or completed transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to			"Network adapters involved	
bit or bit configuration that may be inspected to determine a status or condition.  23  24  25  26  27  28  29  29  20  20  20  20  21  22  23  24  25  26  26  27  28  28  29  20  20  20  20  20  20  20  20  20	20	Dictionary of Computing	in the transfer of data	of a data frame transfer. In
may be inspected to determine a status or condition.  23  24  25  26  27  28  may be inspected to determine a status or condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 21; claim 22; claim 23; claim 31;  29  20  21  22  23  24  25  26  27  28  29  29  20  20  20  20  21  22  23  24  25  26  27  28  29  29  20  20  20  21  21  22  23  24  25  26  26  27  28  29  20  20  20  20  21  21  22  23  24  25  26  27  20  21  22  23  24  25  26  27  28  29  20  20  20  21  21  22  23  24  25  26  27  20  21  21  22  23  24  25  26  27  27  28  28  29  20  20  20  21  21  21  22  23  24  25  26  27  20  20  21  21  22  23  24  25  26  27  27  28  28  29  20  20  21  21  22  23  24  25  26  27  20  20  21  21  22  23  24  25  26  27  27  28  28  29  20  20  20  20  21  21  21  21  22  23  24  25  26  27  20  20  20  21  21  21  21  22  23  24  25  26  27  20  20  21  21  21  21  22  23  24  25  25  26  27  27  20  20  20  20  20  20  20  20	21			many circumstances, the
condition.  INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 21; claim 22; claim 23; claim 31;  processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame in the network adapter has received a data frame in the network adapter has allowing transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to other host devices on other host devices of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame host processor may need to device a data frame host processor may need to device a data frame host processor may need to device a data frame host processor may need to device a data frame host processor may need to device a data frame host processor may need to device a data frame host processor	22	may be inspected to	and a host computer system	some action based on a
24 25 26 28 29 29 20 20 20 21 22 23 24 25 26 26 27 28 29 20 20 20 21 21 22 23 24 25 26 26 27 28 28 29 20 20 21 21 22 23 24 24 25 26 27 28 29 20 20 21 21 22 23 24 24 25 26 27 26 27 27 28 28 29 20 20 21 21 22 23 24 24 25 26 27 28 28 29 29 20 20 21 21 22 23 24 25 26 27 28 29 20 20 21 21 22 23 24 24 25 26 27 28 29 20 20 21 21 21 22 23 24 24 25 26 26 27 27 28 28 29 20 20 21 21 21 22 23 24 24 26 26 27 28 28 28 28 28 28 28 28 28 28 28 28 28	22			completed transfer of a data
Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 21; claim 22; claim 23; claim 31;  Claims: see, e.g., claim 12 some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to other host devices on other h	23	condition.	of a data frame transfer. In	network adapter has
25 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 21; claim 22; claim 23; claim 31; some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to other host devices on a completed transfer of a data frame, the host processor may need to other host devices on other host dev	24		1	received a data frame, the
signal"); see also claim 1; claim 17; claim 19; claim 21; claim 22; claim 31; claim 31; frame. For example, if the network adapter has received a data frame, the host processor may need to other host devices on	27			view the data frame resident
claim 5; claim 13; claim 17; network adapter has received a data frame, the 22; claim 23; claim 31; network adapter has received a data frame, the host processor may need to other host devices or	25	includes an early receive		in the network adapter
claim 19; claim 21; claim received a data frame, the 22; claim 23; claim 31; host processor may need to other host devices of	26			allowing transfer of the data
		claim 19; claim 21; claim	received a data frame, the	frame to host memory or
	27			other host devices on the computer system bus.
28	28	1 , , , , , , , , , , , , , , , , , , ,		<u> </u>

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supportin
	evidence	evidence	evidence
	40; claim 41; claim 44;	in the network adapter	Moreover, if a
	claim 45; claim 50; claim	buffer memory before	determination is made that
	51; claim 52; claim 53;	allowing transfer of the data	the data frame will be
	Specification: see, e.g., col.	frame to host memory or	transferred to the host
	2:35-38 ("The apparatus is	other host devices on the	computer system, the host
	coupled between a network	computer system bus.	processor may require
	transceiver and a host	Moreover, if a	notification of the
	system which includes a	determination is made that	completion of the transfer
	host processor and host	the data frame will be	the data frame from the
	memory.");col. 2:52-54	transferred to the host	network adapter buffer
	("The indication signal to	computer system, the host	memory to the host
	the host is generated based	processor may require	computer system.
	on the comparison of the	notification of the	
	counter and the threshold	completion of the transfer of	Likewise, with respect to
	value in the alterable storage	the data frame from the	the transmission path, the
	location"); col. 3:7-11	network adapter buffer	host processor may require
	("According to another	memory to the host	notification on the
	aspect of the present	computer system.	completion of a data frame
	invention, the network	January System.	transfer. The host process
	interface logic includes	"Likewise, with respect to	may require notification o
	control means for	the transmission path, the	the completion of a
	generating an interrupt	host processor may require	download of a data frame
	signal to the host processor	notification on the	from a host system to the
	responsive to the indication	completion of a data frame	network adapter buffer
	signal."); col. 3:33-4:12	transfer. The host processor	memory. In addition, a
	("According to yet another	may require notification of	notification to the host
	aspect of the present	the completion of a	processor on the completic
	invention, the network	download of a data frame	of the transmission of a da
	adapter includes look-ahead	from a host system to the	frame from the network
	threshold logic for	network adapter buffer	adapter buffer memory on
	generating an early receive	memory. In addition, a	the communications
	indication signal during the	notification to the host	network may be required.
	receiving of the data frame.	processor on the completion	network may be required.
	The data frame includes a	of the transmission of a data	In prior ant systems such
	header field followed by a	frame from the network	<i>In prior art systems</i> , such the National Semiconduct
	data field. The look-ahead	adapter buffer memory onto	DP83932B, a systems-
	threshold logic includes an	the communications	oriented network interface
	alterable storage location	network may be required.	controller (SONIC) and th
	containing a look-ahead	network may be required.	Intel 82586 local area
	threshold value representing	"In prior art systems, such	network co-processor, an
	an amount of data relative to	as the National	interrupt is generated by t
	the beginning of the header	Semiconductor DP83932B,	network adapter to the ho
			processor on the completi
	field. A comparison between the look-ahead	a systems-oriented network interface controller	
			of a data transfer. The hos
	threshold value in the	(SONIC) and the Intel	processor then must
	alterable storage location	82586 local area network	determine the cause of the
	and the counter generates an	co-processor, an interrupt is	interrupt by examining the
	early receive indication	generated by the network	appropriate network adapt
	signal. View logic is also	adapter to the host	status registers and take th
	provided to present the data	processor on the completion	appropriate action.
	frame in the buffer memory	of a data transfer. The host	However, before the host
	to the host system prior to	processor then must	processor services the
	transferring to the host	determine the cause of the	interrupt, the host process

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	memory. Yet, according to	interrupt by examining the	must save its current
	another aspect of the present	appropriate network adapter	environment or system
	invention, the network	status registers and take the	parameters. This routine o
	adapter includes length-left	appropriate action.	saving the host processor's
	threshold logic for	However, before the host	current environment may
	generating a receive	processor services the	take as long as 30 .µs for a
	complete indication signal	interrupt, the host processor	OS/2 operating system. The
	during the receiving of the	must save its current	period of time necessary f
	data frame which includes a	environment or system	saving the host processor's
	header field followed by a	parameters. This routine of	environment depends upo
	data field. The length-left	saving the host processor's	the type of host processor
	threshold includes an	current environment may	used, the host computer
	alterable storage location	take as long as 30 .mu.s for	system configuration and
	containing a length-left	a OS/2 operating system.	when the interrupt
	threshold value representing	The period of time	/occurred.
	an amount of data relative to	necessary for saving the	
	the end of the data field. A	host processor's	As can be seen, there is
	comparison of the length-	environment depends upon	interrupt latency between
	left threshold value in the	the type of host processor	when the network adapter
	alterable storage location	used, the host computer	has completed a transfer
	and the counter generates an	system configuration and	and when the host process
	early receive indication	when the interrupt	is able to service the
	signal. Also, error detection	/occurred.	interrupt generated by the
	means is provided for		network adapter. In essen
	checking the data field	"As can be seen, there is	the host system/network
	transferred from the	interrupt latency between	adapter performance is in
	network transceiver to the	when the network adapter	idle state even though a
	buffer memory which	has completed a transfer	transfer has been complet
	generates a receive frame	and when the host processor	because the host processo
	status signal. According to	is able to service the	is saving its current
	another aspect of the present	interrupt generated by the	environment. For example
	invention, the network	network adapter. In essence,	a data frame may have be
	adapter includes transfer	the host system/network	received and is resident in
	threshold logic for	adapter performance is in an	the network adapter buffe
	generating a transfer	idle state even though a	memory for as long as 30
	complete indication signal	transfer has been completed	before the host processor
	during the transferring of	because the host processor	able to determine the caus
	the data frame from the	is saving its current	of the interrupt and view
	network buffer memory to	environment. For example,	data frame.
	the host system. The	a data frame may have been	
	network buffer memory	received and is resident in	The host system/network
	being independent from the	the network adapter buffer	adapter performance
	host address space. The	memory for as long as 30	degradation introduced by
	transfer threshold logic	.mu.s before the host	interrupt latency is
	includes an alterable storage	processor is able to	compounded when multip
	location containing a	determine the cause of the	data frames are transferre
	transfer threshold value	interrupt and view the data	Between each data frame
	representing an amount of	frame.	transfer, there will be an
	the data frame to be		embedded delay period
	transferred before	"The host system/network	when the network adapter
	generating a transfer	adapter performance	waiting for the host
	complete indication."); see	degradation introduced by	processor to save its curre
	<u>also</u> col. 1:20-2:27; col.	interrupt latency is	environment and respond

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	41:44-50; col. 42:17-25; col.	compounded when multiple	a network adapter interrup
	2:29-41; col. 6:9-59; col.	data frames are transferred.	signal.
	5:68-6:22; col. 2:22-26; col.	Between each data frame	<b>D</b> 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
	2:30-39; col. 2:43-50; col.	transfer, there will be an	Performance degradation i
	3:8-11; col. 3:15-18; col.	embedded delay period	further complicated by the
	3:22-36; col. 3:41-43; col.	when the network adapter is	dynamic nature of interrup
	3:47-51; col. 3:54-57; col.	waiting for the host	latency. While interrupt latency is relatively consta
	3:61-65; col. 4:3-7; col. 6:10-15; col. 6:34-40; col.	processor to save its current environment and respond to	given a periodic interrupt,
	6:48-60; col. 29:31-39; col.	a network adapter interrupt	interrupt latency may
	29:64-66; col. 30:10-13; col.	signal.	increase substantially in th
	34:26-28; col. 42:17-19; see	Signai.	form of spikes depending
	also Prosecution History:	"Performance degradation is	upon when the interrupt
	Notice of Allowability, Oct.	further complicated by the	occurred. Moreover, the
	14, 1993, pp. 2-3.	dynamic nature of interrupt	host computer system
	,, pp	latency. While interrupt	configuration may be
	EXTRINSIC EVIDENCE:	latency is relatively constant	altered by installation of
	3Com's expert, Dr. Michael	given a periodic interrupt,	additional software or
	Mitzenmacher may provide	interrupt latency may	devices on the system bus
	an expert report or other	increase substantially in the	which will increase interru
	form of testimony regarding	form of spikes depending	latency.
	the technology to which this	upon when the interrupt	
	term relates and how a	occurred. Moreover, the	Therefore, it is desirable to
	person having ordinary skill	host computer system	provide a network adapter
	in the art in the field of	configuration may be	with an optimized indication
	networking technology	altered by installation of	signal to the host processo
	would understand this term.	additional software or	of the completion of the
	3Com reserves the right to	devices on the system bus	transfer of a data frame
	rely on testimony by any	which will increase interrupt	which reduces interrupt
	expert in this action.	latency.	latency allowing for
	See also U.S. Patent Nos.	"Therefore, it is desirable to	optimized network adapter/host system
	5,434,872; 5,732,094;	provide a network adapter	performance.")
	6,327,625; 6,526,446; and	with an optimized indication	perjormance.
	6,570,884; Joint Claim	signal to the host processor	'459 patent at 2:29-41 ("T
	Construction Statement in	of the completion of the	present invention provides
	Cv-05-00098 (VRW).	transfer of a data frame	for optimized indication
		which reduces interrupt	signals to a host processor
	3Com reserves the right to	latency allowing for	by a network adapter of th
	rely on any statement made	optimized network	completion of a transfer of
	by any party under the	adapter/host system	data frame. The apparatus
	Patent Local Rules.	performance." ('459	coupled between a networ
		col.1:20-2:27).	transceiver and a host
			system which includes a
		"The present invention	host processor and host
		provides for optimized	memory. The apparatus
		indication signals to a host	generates an indication
		processor by a network	signal to the host processo
		adapter of the completion of	responsive to the transfer of
		a transfer of a data frame.	a data frame. The host
		The apparatus is coupled	processor responds to the
		between a network	indication signal after a
	1	transceiver and a host	period of time. The

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		system which includes a	apparatus includes network
		host processor and host	interface logic for
		memory. The apparatus	transferring the data frame
		generates an indication	between the network
		signal to the host processor	transceiver and a buffer
		responsive to the transfer of a data frame. The host	memory for storing the data frame.")
		processor responds to the	mame. )
		indication signal after a	'459 patent at 6:9-59
		period of time. The	("Threshold logic 10 in
		apparatus includes network	network adapter 3 is
		interface logic for	designed for eliminating or
		transferring the data frame	reducing interrupt latency.
		between the network	Threshold logic 10 makes a
		transceiver and a buffer	determination of how much
		memory for storing the data	of a data frame is
		frame." ('459 col. 2:29-41)	transferred before
			generating an early
		"Typically, devices on host	indication signal. The early
		bus 4, such as network	indication signal may then
		adapter 3, request service	cause an early interrupt
		from host processor 5 by	signal to be generated
		generating an interrupt on	during the transfer of a dat
		host bus 4. The host	frame. Moreover, threshold
		processor 5 then must save	logic 10 is designed such
		its system parameters and determine which device	that the time required for transferring the remainder
		caused the interrupt and	of the data frame should
		what service is required.	approximately equal the
		Interrupt latency is	time required for host
		introduced from when a	processor 5 save its system
		device such as network	parameters. Therefore,
		adapter 3 generates an	interrupt latency is
		interrupt signal and when	eliminated or reduced by
		host processor 5 is able to	allowing host processor 5's
		service the device.	interrupt routine to coincide
			with the transfer of the
		"Threshold logic 10 in	remainder of the data frame
		network adapter 3 is	Tro 2: 0 : 111 1
		designed for eliminating or	FIG. 2 is a functional block
		reducing interrupt latency.	diagram of network adapter
		Threshold logic 10 makes a determination of how much	3 with threshold logic 10
		of a data frame is	illustrating the various
		transferred before	transfer paths. Network adapter 3 contains
		generating an early	transceiver 12 which
		indication signal. The early	transmits and receives data
		indication signal may then	frames across network 2.
		cause an early interrupt	Network interface logic 11
		signal to be generated	is responsible for the
		during the transfer of a data	transfer of a data frame
		frame. Moreover, threshold	between network buffer 9
	İ	logic 10 is designed such	and transceiver 12.

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		that the time required for transferring the remainder	Likewise, the network
		of the data frame should	adapter 3 contains host interface logic 8 which is
		approximately equal the	responsible for transferring
		time required for host	a data frame between
		processor 5 save its system	network buffer 9 and host
		parameters. Therefore,	system 1. Threshold logic
		interrupt latency is	10 contains an alterable
		eliminated or reduced by	storage location 10a which
		allowing host processor 5's	contains a threshold value.
		interrupt routine to coincide with the transfer of the	This threshold value
		remainder of the data	represents the amount of a data frame which will be
		frame." ('459 col. 5:68-	transferred into or out of
		6:22).	buffer 9 before an early
		<del>-),</del>	indication signal will be
		"Therefore, the present	generated which may cause
		invention reduces host	host interface logic 8 to
		processor interrupt latency	send an interrupt to host
		by generating early	processor 5. Host processor
		indications of data frame transfers. These early	5 has access to the alterable
		indications then may be	storage 10a location containing the threshold
		used to generate an early	value through host interface
		interrupt to the host	logic 8.
		processor before the data	8
		frame is transferred which	The threshold logic also
		allows the host processor to	includes a means for the
		save its current environment	host processor 5 to
		during a data frame	dynamically alter the time a
		transfer." ('459, col. 41:44- 50).	which an indication is generated based on prior
		30).	host processor 5 responses.
		"The above indication	When responding to an
		signals are further optimized	interrupt generated by an
		by allowing the host	early indication, the host
		processor to dynamically	processor may examine
		tune the timing of the	network adapter status
		indication signals. The host	information to determine if
		processor has write access to the threshold registers	host processor 5 is servicing the interrupt too early or too
		and may alter the threshold	late. If host processor 5
		values in the threshold	responds to network adapte
		registers based on posted	3 before a complete data
		status information by the	frame is transferred, host
		network adapter. The posted	processor 5 then may
		status information will	decrease the threshold value
		allow the host processor to	in alterable storage location
		determine whether it is	10a enabling threshold logic
		responding too early or too	10 to generate the indication signal at a later time in the
		late to an interrupt generated by the	next transfer of a data
		indications." ('459, col.	frame. Alternatively, if hos

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
	evidence	42:17-25, emphasis added.)	processor 5 responds to the
		D//	network adapter 3 after a
		DICTIONARY/TREATISE DEFINITIONS:	complete data frame has already been transferred,
		DEFINITIONS.	host processor 5 may then
		Webster's Third New	increase the threshold value
		International Dictionary Unabridged (1981):	in alterable storage location 10a enabling the threshold
		something (as a signal)	logic to generate an
		that serves to indicate	indication signal at an
		Evenes Teamy cover	earlier time in the next
		EXPERT TESTIMONY:	transfer of a data frame.")
		D-Link's expert, Howard	'459 patent at 5:68-6:22
		Frazier, may provide testimony as to the	("Typically, devices on host bus 4, such as network
		definition of the disputed	adapter 3, request service
		terms as would be	from host processor 5 by
		understood by one of ordinary skill in the relevant	generating an interrupt on host bus 4. The host
		art and may provide an	processor 5 then must save
		explanation of the	its system parameters and
		technology.	determine which device caused the interrupt and
		D-Link also incorporates by	what service is required.
		reference Realtek's cited	Interrupt latency is
		references.	introduced from when a device such as network
			adapter 3 generates an
			interrupt signal and when
			host processor 5 is able to service the device.
			service the device.
			Threshold logic 10 in
			network adapter 3 is designed for eliminating or
			reducing interrupt latency.
			Threshold logic 10 makes a
			determination of how much of a data frame is
			transferred before
			generating an early
			indication signal. The early indication signal may then
			cause an early interrupt
			signal to be generated
			during the transfer of a data frame. Moreover, threshold
			logic 10 is designed such
			that the time required for
			transferring the remainder of the data frame should
			approximately equal the

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
3				time required for host processor 5 save its system
4				parameters. Therefore, interrupt latency is
5				eliminated or reduced by allowing host processor 5's interrupt routine to coincide
6				with the transfer of the remainder of the data
7				frame.")
8				'459 patent; at 41:44-50 ("Therefore, the present
9				invention reduces host processor interrupt latency by generating early
10				indications of data frame transfers. These early
11 12				indications then may be used to generate an early interrupt to the host
13				processor before the data frame is transferred which
14				allows the host processor to save its current environment
15				during a data frame transfer.")
16				<u>Dictionary/treatise</u>
17				DEFINITIONS: signal
18				Newton's' Telecom Dictionary (fourth edition,
19 20				1991) Signal: 1. An electrical
21				wave used to convey information 2. An alert. 3.
22				An acoustic device (e.g. a bell) or a visual device (e.g. a lamp) which calls
23				attention. To transmit an information signal or
24				alerting signal.
25				McGraw Hill Electronics Dictionary (fifth edition, 1994)
26				Signal: Any variation in an electrical current, visible or
27				nonvisible light, audible or ultrasonic energy that
28		1		0,

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
			conveys information.
			Signals can be coded in
			frequency, phase, or
			amplitude to separate them
			from unwanted noise.
			EXPERT TESTIMONY:
			Realtek's expert, Dr. Izhak
			Rubin, may provide
			testimony as to the
			definition of the disputed
			terms as would be
			understood by one of
			ordinary skill in the relevan
			art and may provide an
			explanation of the
			technology.
"logic"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	Please refer to the
	Circuitry and/or		construction under 35
found in claim	programming.	When used as a standalone	U.S.C. § 112 ¶ 6 for the
numbers:		term in the claims, "logic" is	separate claim limitations of
	DICTIONARY/TREATISE	an unspecified claim	the separate claims. To the
'459 patent: 1	DEFINITIONS: Synopsis, Inc.,	element defined only by its	extent this term requires
	Electronic Design	function and thus requires	construction, Realtek asser
also presented for	Automation Glossary of	interpretation under invokes	that "logic" (or "logic for"
construction in:	Terms, at	35 U.S.C. § 112 ¶ 6.	should be construed as
(070	http://www.synopsis.com/ne	T	"means" (or "means for")
'872 patent: 1, 21	ws/pr_kit/eda_glossry.html:	In computer software or hardware context, "means"	and, therefore, the associated claim elements
'625 patent: 23	The sequence of functions performed by hardware or	or "means for."	
623 patent. 25	software. Hardware logic is	of means for.	should be governed by 35 U.S.C. § 112 ¶ 6. If the
'884 patent: 1	made up of circuits that	See discussion in section	Court determines that 35
884 patent. 1	perform an operation.	below concerning 35 U.S.C.	U.S.C. § 112 ¶ 6 does not
	Software logic is the	§ 112 ¶ 6 constructions for	apply, "logic" should be
	sequence of instructions in a	phrases including "logic."	construed as "device."
	program; see also IBM	pinuses meruanig regie.	construct as device.
	Dictionary of Computing	D-Link also incorporates by	DICTIONARY/TREATISE
	(10th ed. 1993): The	reference Realtek's	DEFINITIONS:
	systematized	references.	
	interconnection of digital		Synopsis, Inc., Electronic
	switching functions,		Design Automation
	circuits, or devices;		Glossary of Terms
	Microsoft Computer		The sequence of functions
	Dictionary (5th ed. 2002):		performed by hardware or
	In programming, the		software. Hardware logic i
	assertions, assumptions, and		made up of circuits that
	operations that define what		perform an operation.
	a given program does.		Software logic is the
	Defining the logic of a		sequence of instructions in
	program is often the first		program.
	step in developing the		

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
		program's source code.		Newton's Telecom
3		INTRINSIC EVIDENCE:		<u>Dictionary</u> :
4		Claims: claim 1; claim 2;		"Logica system that could be applied to the
_		claim 3; claim 4; claim 5;		relationships between
5		claim 11; claim 22; claim 24; claim 30; claim 34;		propositions to which only a
6		claim 38; claim 40; claim		binary choice of truth existed, i.e., yes or no."
Ů		42; claim 44; claim 46;		Calsted, i.e., yes of no.
7		claim 48; claim 50; claim 52; Specification: figs. 1, 2,		IBM Dictionary of
8		5, 9, 11; col. 2:38-39; col.		Computing (10th ed. 1993): The systematized
0		2:41-50; col. 2:55-3:11; col.		interconnection of digital
9		3:15-22; col. 3:25-28; col. 3:33-38; col. 3:44-51; col.		switching functions,
1.0		3:61-65; col. 3:67-4:11; col.		circuits, or devices.
10		4:21-23; col. 4:50-51; col.		EXPERT TESTIMONY:
11		5:50-54; col. 5:56-58; col. 6:9-13; col. 6:15-19; col.		
		6:23-25; col. 6:27-44; col.		Realtek's expert, Dr. Izhak Rubin, may provide
12		6:48-59; col. 7:41-43; col.		testimony as to the
13		9:4-6; col. 10:30-33; col. 10:42-45; col. 12:58-61; col.		definition of the disputed
13		12:30-37; col. 12:39-43; col.		terms as would be
14		12:50-58; col. 12:60-65; col.		understood by one of ordinary skill in the relevant
15		13:12-14; col. 14:1-4; col. 18:4-18; col. 18:27-30; col.		art and may provide an
13		18:35-40; col. 18:47-51; col.		explanation of the
16		18:62-19:9; col. 19:14-17;		technology.
		col. 19:19-23; col. 19:42-47; col. 19:55-59; col. 24:17-25;		
17		col. 24:34-36; col. 24:38-40;		
18		col. 24:48-59; col. 24:62-68;		
		col. 25:11-24; col. 25:41-47; col. 25:53-68; col. 26:1-18;		
19		col. 26:29-34; col. 29:33-39;		
20		col. 29:59-67; col. 30:10-13;		
20		col. 30:15-41; col. 30:49-52; col. 30:56-58; col. 31:25-28;		
21		col. 31:31-40; col. 31:50-52;		
22		col. 32:2-4; col. 32:15-22;		
		col. 32:50-55; col. 33:59-62; col. 33:64-67; col. 34:25-32;		
23		col. 37:23-26; col. 37:42-46;		
24		col. 38:12-22; col. 39:55-57;		
24		col. 41:51-55; col. 41:65; col. 41:67-42:2; col. 42:5-		
25		16; see also Prosecution		
		History: Notice of		
26		Allowability, Oct. 14, 1993, pp. 2-3.		
27		PP. 2 3.		
		EXTRINSIC EVIDENCE:		
28				

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	3Com's expert, Dr. Michael		
	Mitzenmacher may provide		
	an expert report or other		
	form of testimony regarding		
	the technology to which this term relates and how a		
	person having ordinary skill		
	in the art in the field of		
	networking technology		
	would understand this term.		
	3Com reserves the right to		
	rely on testimony by any		
	expert in this action.		
	See also U.S. Patent Nos.		
	5,434,872; 5,732,094;		
	6,327,625; 6,526,446; and 6,570,884; Joint Claim		
	Construction Statement in		
	Cv-05-00098 (VRW).		
	3Com reserves the right to		
	rely on any statement made		
	by any party under the		
"threshold value"	Patent Local Rules.	Dropogra governversov	Dronoger governversov
threshold value	PROPOSED CONSTRUCTION: A value representing the	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
found in claim	quantity of data sufficient to	A set value indicating a desired limit.	A number corresponding to a level of data required for
numbers:	trigger the initiation of some	desired iiiiit.	some process to take place.
	process	REFERENCES:	
'459 patent: 1			DICTIONARY/TREATISE
	DICTIONARY/TREATISE	PATENT SPECIFICATION:	DEFINITIONS:
also presented for	<u>DEFINITIONS</u> : <u>threshold</u> : <u>The</u>	"If host processor 5	<u>threshold</u>
construction in:	American Heritage	responds to network adapter	
(072	Dictionary of the English	3 before a complete data	The American Heritage
'872 patent: 10	Language (4th ed. 2000): The point that must be	frame is transferred, host processor 5 then may	Dictionary of the English Language (4th ed. 2000):
'094 patent: 47	exceeded to begin	decrease the <i>threshold value</i>	The point that must be
or patent. Tr	producing a given effect or	in alterable storage location	exceeded to begin
	result or to elicit a response;	10a enabling threshold logic	producing a given effect or
	see also Dictionary of	10 to generate the indication	result or to elicit a response
	<u>Computing</u> (1st ed. 1983):	signal at a later time in the	
	Threshold element: A logic	next transfer of a data	McGraw-Hill Electronics
	element whose output is	frame. Alternatively, if host	Dictionary (fifth edition,
	determined by comparing a	processor 5 responds to the	1994) Through ald, 1. The least
	weighted sum of inputs with a predetermined/prescribed	network adapter 3 after a complete data frame has	Threshold: 1. The least value of a current, voltage,
	threshold value. If the	already been transferred,	or other quantity that
	threshold is exceeded, the	host processor 5 may then	produces the minimum
	output is a logic 1; if not,	increase the threshold value	detectable response. It is
	the output is logic 0. If the	in alterable storage location	also called a limen. 2. The
	number of inputs is odd, if	10a enabling the threshold	level of pumping at which
		logic to generate an	laser can go into self-excite

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_	<b>-</b>			
1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
ااد	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence oscillation.
3		and the threshold is equal to half of the number of inputs,	indication signal at an earlier time in the next	oscination.
3		then the threshold element	transfer of a data frame."	threshold value
4		behaves as a majority	('459; Col. 6: 48-59)	threshold value
7		element. A system of	(emphasis added).	McGraw-Hill Electronics
5		threshold elements is	(	Dictionary (fifth edition,
~ <b> </b>		described by or as threshold	"The above indication	1994)
6		logic.	signals are further optimized	Threshold Value: The
			by allowing the host	minimum input that
7		INTRINSIC EVIDENCE:	processor to dynamically	produces a corrective action
		Claims: claim 1; claim 5;	tune the timing of the	in an automatic control
8		claim 8; claim 9; claim 10; claim 15; claim 16; claim	indication signals. The host processor has write access	system.
		18; claim 20; claim 22;	to the threshold registers	EXPERT TESTIMONY:
9		claim 23; claim 27; claim	and may alter the <i>threshold</i>	DATERT TESTIMONT.
1.0		28; claim 29; claim 33;	values in the threshold	Realtek's expert, Dr. Izhak
10		claim 34; claim 35; claim	registers based on posted	Rubin, may provide
11		36; claim 37; claim 40;	status information by the	testimony as to the
11		claim 41; claim 44; claim	network adapter. The	definition of the disputed
12		45; claim 50; claim 51;	posted status information	terms as would be
12		claim 52; claim 53; <u>Specification</u> : see, e.g., fig.	will allow the host processor to determine whether it is	understood by one of ordinary skill in the relevant
13		2; col. 3:67-4:2 ("The	responding too early or too	art and may provide an
		transfer threshold logic	late to an interrupt generated	explanation of the
14		includes an alterable storage	by the indications." ('459;	technology.
		location containing a	Col. 42: 17-25) (emphasis	
15		transfer threshold value	added).	
1.0		representing an amount of the data frame to be	"The control manner also	
16		transferred before	"The control means also posts status information	
17		generating a transfer	which may be used by the	
1 /		complete indication"); see	host processor as feedback	
18		also col. 2:46-50; col. 2:52-	for optimizing the <i>threshold</i>	
		54; col. 3:11-14; col. 3:18-	value in the alterable	
19		25; col. 3:28-32; col. 3:37-	storage location." ('459;	
		46; col. 3:51-57; col. 4:7-11; col. 4:50-51; col. 6:32-40;	Col. 3: 11-14) (emphasis added).	
20		col. 6:48-59; col. 21:40-42;	added).	
_,		col. 30:15-25; col. 30:45-48;	"Threshold logic 10 in	
21		col. 30:49-52; col. 31:19-22;	network adapter 3 is	
22		col. 32:6-8; col. 32:13-15;	designed for eliminating or	
22		col. 32:37-39; col. 35:39-41;	reducing interrupt latency.	
23		col. 35:43-45; col. 35:52-56;	Threshold logic 10 makes a	
		col. 36:45-47; col. 39:66-67; col. 40:26-32; col. 41:51-55;	determination of how much of a data frame is	
24		col. 41:67-42:4; col. 42:19-	transferred before	
		22; Col. 42: 17-25; Col. 1:	generating an early	
25		46-51; Col. 1: 63-66; Col. 2:	indication signal. The early	
ار آ		46-54; Col. 2: 30-35; Col. 2:	indication signal may then	
26		23-27; Col. 41: 44-55; 459;	cause an early interrupt	
27		Col. 6: 9-59; Col. 3: 11-14; see also Prosecution	signal to be generated	
27		History: Notice of	during the transfer of a data frame. Moreover, threshold	
28		<u> </u>	mame. moreover, uneshold	
20				

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	Allowability, Oct. 14, 1993,	logic 10 is designed such	
	pp. 2-3.	that the time required for	
	EXTRINSIC EVIDENCE:	transferring the remainder of the data frame should	
	3Com's expert, Dr. Michael	approximately equal the	
	Mitzenmacher may provide	time required for host	
	an expert report or other	processor 5 save its system	
	form of testimony regarding	parameters. Therefore,	
	the technology to which this	interrupt latency is	
	term relates and how a	eliminated or reduced by	
	person having ordinary skill	allowing host processor 5's	
	in the art in the field of	interrupt routine to coincide	
	networking technology	with the transfer of the	
	would understand this term.	remainder of the data frame.	
	3Com reserves the right to	FIG. 2 is a functional block	
	rely on testimony by any	diagram of network adapter	
	expert in this action.	3 with threshold logic 10	
	Can also II C. Data 4 N	illustrating the various	
	See also U.S. Patent Nos.	transfer paths. Network	
	5,434,872; 5,732,094; 6,327,625; 6,526,446; and	adapter 3 contains transceiver 12 which	
	6,570,884; Joint Claim	transmits and receives data	
	Construction Statement in	frames across network 2.	
	Cv-05-00098 (VRW).	Network interface logic 11	
	( V 03 000)0 ( V I V V ).	is responsible for the	
	3Com reserves the right to	transfer of a data frame	
	rely on any statement made	between network buffer 9	
	by any party under the	and transceiver 12.	
	Patent Local Rules.	Likewise, the network	
		adapter 3 contains host	
		interface logic 8 which is	
		responsible for transferring	
		a data frame between	
		network buffer 9 and host	
		system 1. Threshold logic 10 contains an alterable	
		storage location 10a which	
		contains a threshold value.	
		This threshold value	
		represents the amount of a	
		data frame which will be	
		transferred into or out of	
		buffer 9 before an early	
		indication signal will be	
		generated which may cause	
		host interface logic 8 to	
		send an interrupt to host	
		processor 5. Host processor	
		5 has access to the alterable	
		storage 10a location	
		containing the <i>threshold</i>	
		value through host interface	
		logic 8. The threshold logic	1

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		also includes a means for	
		the host processor 5 to dynamically alter the time at	
		which an indication is	
		generated based on prior	
		host processor 5 responses.	
		When responding to an	
		interrupt generated by an	
		early indication, the host	
		processor may examine	
		network adapter status	
		information to determine if	
		host processor 5 is servicing	
		the interrupt too early or too late. If host processor 5	
		responds to network adapter	
		3 before a complete data	
		frame is transferred, host	
		processor 5 then may	
		decrease the threshold value	
		in alterable storage location	
		10a enabling threshold logic	
		10 to generate the indication	
		signal at a later time in the	
		next transfer of a data	
		frame. Alternatively, if host processor 5 responds to the	
		network adapter 3 after a	
		complete data frame has	
		already been transferred,	
		host processor 5 may then	
		increase the threshold value	
		in alterable storage location	
		10a enabling the threshold	
		logic to generate an	
		indication signal at an earlier time in the next	
		transfer of a data frame."	
		('459; Col. 6: 9-59)	
		(emphasis added).	
		"Therefore, the present	
		invention reduces host	
		processor interrupt latency	
		by generating early	
		indications of data frame	
		transfers. These early indications then may be	
		used to generate an early	
		interrupt to the host	
		processor before the data	
		frame is transferred which	
		allows the host processor to	•

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
	evidence	save its current environment	evidence
		during a data frame transfer.	
		The early indications are	
		generated by threshold logic	
		which determines how	
		much of a data frame is	
		transferred before	
		generating an early	
		indication by comparing a	
		threshold value in a	
		threshold register to a data	
		transfer counter." ('459; Col. 41: 44-55) (emphasis	
		added).	
		added).	
		"Therefore, it is desirable	
		to provide a network adapter	
		with an optimized indication	
		signal to the host processor	
		of the completion of the	
		transfer of a data frame which reduces interrupt	
		latency allowing for	
		optimized network	
		adapter/host system	
		performance." ('459; Col.	
		2: 23-27).	
		((77)	
		"The present invention	
		provides for optimized indication signals to a host	
		processor by a network	
		adapter of the completion of	
		a transfer of a data frame.	
		The apparatus is coupled	
		between a network	
		transceiver and a host	
		system which includes a	
		host processor and host memory." ('459; Col. 2:	
		30-35).	
		"The threshold logic	
		includes a counter coupled	
		to the buffer memory for	
		counting the data transfer to	
		or from the buffer memory, and an alterable storage	
		location containing a	
		threshold value. Means for	
		comparing the counter and	
		the alterable storage	
		location is also provided.	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting evidence
	evidence	<ul><li>evidence</li><li>The indication signal to the</li></ul>	evidence
		host is generated based on	
		the comparison of the	
		counter and the threshold	
		<i>value</i> in the alterable storage	
		location." ('459; Col. 2: 46-	
		54) (emphasis added).	
		"As can be seen, there is	
		interrupt latency between	
		when the network adapter	
		has completed a transfer and	
		when the host processor is able to service the interrupt	
		generated by the network	
		adapter." ('459; Col. 1: 63-	
		66).	
		"In prior art systems, such	
		as the National	
		Semiconductor DP83932B,	
		a systems-oriented network	
		interface controller (SONIC) and the Intel	
		82586 local area network	
		co-processor, an interrupt is	
		generated by the network	
		adapter to the host processor	
		on the completion of a data	
		transfer." ('459; Col. 1: 46-	
		51).	
		EXTRINSIC EVIDENCE:	
		EXPERT TESTIMONY:	
		D-Link's expert, Howard	
		Frazier, may provide	
		testimony as to the definition of the disputed	
		terms as would be	
		understood by one of	
		ordinary skill in the relevant	
		art and may provide an	
		explanation of the	
		technology.	
		DICTIONARY/TREATISE	
		DEFINITIONS:	
		Webster's Ninth New	
		Collegiate Dictionary	
		(1983), pg.229:	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2	evidence	evidence	evidence
3		Threshold - "A level, point, or value above which something is true or will	
1		take place and below which it is not or will not."	
;		D-Link also incorporates by	
5		reference Realtek's references.	
	<u>l</u>	<u> </u>	
3	II S Pat No. 5 /13/1 872		

### <u>U.S. Pat. No. 5,434,872</u>

Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
,	evidence	evidence	evidence
"falls behind"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
	underruns	The absence of a write	A condition in which the
found in claim		signal during a specified	transferring of data by the
numbers:	DICTIONARY/TREATISE	interval.	host interface falls behind
	<u>DEFINITIONS</u> : <u>See</u> " <b>a</b>		the transferring of data by a
'872 patent: 1	condition in which the	INTRINSIC EVIDENCE:	transmit logic.
	means for transferring		
	falls behind the transmit	PATENT SPECIFICATION:	INTRINSIC EVIDENCE:
	<b>logic</b> " for definitions of		
	"falls behind."	"[U]nderrun detector 413	'872 patent at 28:48-29:2
		for detecting a condition in	("According to the present
	<u>INTRINSIC EVIDENCE</u> :	which the transferring of	invention, this transmit data
	Claims: see, e.g., claim 15	data into the transmit data	path includes an underrun
	("an underrun condition in	buffer, or immediate data to	detector 413 for detecting a
	which the host interface	the transmit descriptor	condition in which the
	means in transferring data to	buffer, by the host interface	transferring of data into the
	the buffer memory falls	falls behind the transferring	transmit data buffer, or
	behind the network interface	of data into the transmit data	immediate data to the
	means in transferring data to	path 400 by the transmit	transmit descriptor buffer,
	the transceiver"); claim 25	DMA logic. The underrun	by the host interface falls
	("a condition in which the	detector 413 is controlled by	behind the transferring of
	data transfer circuitry falls	the transmit control logic	data into the transmit data
	behind the medium access	411. The transmit control	path 400 by the transmit
	controller"); see also claim	logic 411 indicates intervals across line 414 during	DMA logic The underrun detector
	1; claim 18; <u>Specification</u> : fig. 18; col. 28:48-29:2	which a transmit write	determines that a transmit
	("According to the present	TXWR signal is expected	write TXWR signal is not
	invention, this transmit data	on line 402. The underrun	present during an expected
	path includes an underrun	detector determines that a	interval of the frame
	detector 413 for detecting a	transmit write TXWR signal	transmission, then a bad
	condition in which the	is not present during an	frame signal is generated on
	transferring of data into the	expected interval of the	line 409")
	transmit data buffer, or	frame transmission, then a	,
	immediate data to the	bad frame signal is	EXPERT TESTIMONY:
	transmit descriptor buffer,	generated on line 409."	
			<u>l</u>

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supportin
	evidence	evidence	evidence
	by the host interface falls	('872; Col. 28: 49-61).	Realtek's expert, Dr. Izhak
	behind the transferring of		Rubin, may provide
	data into the transmit data	PROSECUTION HISTORY:	testimony as to the
	path 400 by the transmit	- 4 10-2	definition of the disputed
	DMA logic. The underrun	In the '872 prosecution	terms as would be
	detector 413 is controlled by	history in an Amendment	understood by one of
	the transmit control logic	mailed October 5, 1994,	ordinary skill in the relevan
	411. The transmit control	Applicants amended claim 1	art and may provide an
	logic 411 indicates intervals	to overcome a prior art	explanation of the
	across line 414 on line 402.	reference. Applicants	technology.
	The underrun detector determines that a transmit	added, <i>inter alia</i> , the	
		following phrase to claim 1:	
	write TXWR signal in not	"means for transferring falls	
	present during an expected interval of the frame	behind the transmit logic	
	transmission, then a bad	." (See '872 Prosecution	
	frame signal is generated on	History, Amendment mailed	
	line 409. In response to the	October 5, 1994, p. 3).	
	bad frame signal, the CRC	EXTRINSIC EVIDENCE:	
	data is inverted by the	EXTRINSIC EVIDENCE.	
	exclusive OR gate 407	EXPERT TESTIMONY:	
	which causes a bad CRC to	EXIEKT TESTIMONT,	
	be generated for the already	D-Link's expert, Howard	
	transmitted portions of the	Frazier, may provide	
	frame suffering the	testimony as to the	
	underrun. Transmit control	definition of the disputed	
	logic 411 also responds to	terms as would be	
	the bad frame signal on line	understood by one of	
	409 to select the bad CRC	ordinary skill in the relevant	
	data through multiplexer	art and may provide an	
	410. Finally, the bad frame	explanation of the	
	signal on line 409 in used	technology.	
	for posting status		
	information through the		
	xmitFailureRegister of an		
	underrun condition."); Col.		
	28:48-29:2; <u>see also</u>		
	Prosecution History: Office		
	Action, Oct. 26, 1993, p. 3; Response to Office Action,		
	Oct. 5, 1994, p. 2.		
	Oct. 3, 1994, p. 2.		
	EXTRINSIC EVIDENCE:		
	3Com's expert, Dr. Michael		
	Mitzenmacher may provide		
	an expert report or other		
	form of testimony regarding		
	the technology to which this		
	term relates and how a		
	person having ordinary skill		
	in the art in the field of		
	networking technology		

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supportin
	evidence	evidence	evidence
	3Com reserves the right to		
	rely on testimony by any		
	expert in this action.		
	See also U.S. Patent Nos.		
	5,434,872; 5,732,094;		
	6,327,625; 6,526,446; and 6,570,884, (in particular,		
	dependent claims 4 and 6 of		
	the '094); Joint Claim		
	Construction Statement in		
	Cv-05-00098 (VRW).		
	(1111).		
	3Com reserves the right to		
	rely on any statement made		
	by any party under the		
	Patent Local Rules.		
"a condition in which	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
the means for	A transmission underrun	"Means for transferring"	A condition in which the
transferring falls	condition.	requires means-plus-function	transferring of data into a
behind the transmit		analysis; see 35 U.S.C.	transmit data buffer by the
logic"	DICTIONARY/TREATISE	112(6) analysis in Section B.	host interface falls behind
C 1: 1:	DEFINITIONS: See "logic"		the transferring of data into
found in claim	below; condition: The	See also "falls behind."	transmit data path by a
numbers:	American Heritage	If congrately construed D	transmit logic.
'872 patent: 1	Dictionary of the English Language (4th ed. 2000): A	If separately construed, D- Link would propose the	INTRINSIC EVIDENCE:
672 patent. 1	mode or state of being	construction proposed by	INTRINSIC EVIDENCE.
	A state of readiness or	Realtek.	'872 patent at 28:48-29:2
	physical fitness. One that is	reares.	("According to the present
	indispensable to the		invention, this transmit dat
	appearance or occurrence of		path includes an underrun
	another; prerequisite ;		detector 413 for detecting a
	transfer: The American		condition in which the
	Heritage Dictionary of the		transferring of data into the
	English Language (4th ed.		transmit data buffer, or
	2000): The conveyance or		immediate data to the
	removal of something from		transmit descriptor buffer,
	one place, person, or thing		by the host interface falls
	to another. One who		behind the transferring of
	transfers or is transferred, as		data into the transmit data
	to a new school. A design		path 400 by the transmit
	conveyed by contact from		DMA logic The underrun detector
	one surface to another. A		determines that a transmit
	ticket entitling a passenger to change from one public		write TXWR signal is not
	conveyance to another as		present during an expected
	part of one trip. A place		interval of the frame
	where such a change is		transmission, then a bad
	made. Law. A conveyance		frame signal is generated of
	of title or property from one		line 409")
	person to another. <u>fall</u>		, into 107 ,
			EXPERT TESTIMONY
	behind: The American		EXPERT TESTIMONY:

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supports evidence
	Heritage Dictionary of the	evidence	evidence
	English Language (4th ed.		Realtek's expert, Dr. Izha
	2000): To fail to keep up a		Rubin, may provide
	pace; lag behind. transmit:		testimony as to the
	The American Heritage		definition of the disputed
	Dictionary of the English		terms as would be
	Language (4th ed. 2000): To		understood by one of
	send from one person, thing,		ordinary skill in the relevant
	or place to another; convey.		art and may provide an
	See Synonyms at convey.		explanation of the
	See Synonyms at send1. To		technology.
	cause to spread; pass on:		
	transmit an infection. To		
	impart or convey to others		
	by heredity or inheritance; hand down. To pass along		
	(news or information);		
	communicate. Electronics.		
	To send (a signal), as by		
	wire or radio. Physics. To		
	cause (a disturbance) to		
	propagate through a		
	medium. To convey (force		
	or energy) from one part of		
	a mechanism to another. To		
	send out a signal.		
	INTRINSIC EVIDENCE:		
	Claims: see, e.g., claim 15		
	("an underrun condition in		
	which the host interface		
	means in transferring data to		
	the buffer memory falls behind the network interface		
	means in transferring data to		
	the transceiver"); claim 25		
	("a condition in which the		
	data transfer circuitry falls		
	behind the medium access		
	controller"); see also claim		
	1; claim 18; Specification:		
	fig. 18; col. 28:48-29:2		
	("According to the present		
	invention, this transmit data		
	path includes an underrun		
	detector 413 for detecting a		
	condition in which the		
	transferring of data into the		
	transmit data buffer, or		
	immediate data to the		
	transmit descriptor buffer,		
	by the host interface falls		
	behind the transferring of		

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		data into the transmit data	evidence	evidence
3		path 400 by the transmit		
		DMA logic. The underrun		
4		detector 413 is controlled by		
		the transmit control logic		
5		411. The transmit control		
		logic 411 indicates intervals across line 414 on line 402.		
6		The underrun detector		
7		determines that a transmit		
′		write TXWR signal in not		
8		present during an expected		
		interval of the frame transmission, then a bad		
9		frame signal is generated on		
1.0		line 409. In response to the		
10		bad frame signal, the CRC		
11		data is inverted by the		
11		exclusive OR gate 407 which causes a bad CRC to		
12		be generated for the already		
		transmitted portions of the		
13		frame suffering the		
		underrun. Transmit control		
14		logic 411 also responds to		
15		the bad frame signal on line 409 to select the bad CRC		
13		data through multiplexer		
16		410. Finally, the bad frame		
		signal on line 409 in used		
17		for posting status		
1.0		information through the xmitFailureRegister of an		
18		underrun condition."); see		
19		also Prosecution History:		
1)		Office Action, Oct. 26,		
20		1993, p. 3; Response to Office Action, Oct. 5, 1994,		
		p. 2.		
21		F · - ·		
22		EXTRINSIC EVIDENCE:		
22		3Com's expert, Dr. Michael		
23		Mitzenmacher may provide an expert report or other		
		form of testimony regarding		
24		the technology to which this		
ا		term relates and how a		
25		person having ordinary skill		
26		in the art in the field of networking technology		
۷۵		would understand this term.		
27		3Com reserves the right to		
		rely on testimony by any		
28				

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
(anspired terms in even)	evidence	evidence	evidence
	expert in this action.	- Critical Control	- Criwerice
	See also U.S. Patent Nos.		
	5,434,872; 5,732,094;		
	6,327,625; 6,526,446; and		
	6,570,884 (in particular,		
	dependent claims 4 and 6 of		
	the '094); Joint Claim		
	Construction Statement in Cv-05-00098 (VRW).		
	CV-03-00098 (VKW).		
	3Com reserves the right to		
	rely on any statement made		
	by any party under the		
	Patent Local Rules.		
"underrun"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION
c 1: 1:	When expected data from a	The condition of falling	A condition in which the
found in claim numbers:	frame to be transferred is	behind. See proposed construction for "falls	transferring of data into a
numbers:	not available	behind."	transmit data buffer by the host interface falls behind
'872 patent: 1	DICTIONARY/TREATISE	beiling.	the transferring of data into
672 patent. 1	DEFINITIONS: IBM		transmit data path by a
also presented for	Dictionary of Computing		transmit logic.
construction in:	(10th ed. 1993): Loss of		transmit logic.
	data caused by inability of a		INTRINSIC EVIDENCE:
'094 patent: 21	transmitting device or		
1	channel to provide data to		'872 patent at 28:48-29:2
	the communication control		("According to the presen
	logic (SDLC or BSC/SS) at		invention, this transmit da
	a rate that is fast enough for		path includes an underrun
	the attached data link or		detector 413 for detecting
	loop; see also The American		condition in which the
	Heritage Dictionary of the		transferring of data into the
	English Language (4th ed.		transmit data buffer, ,
	2000): Something that runs		the host interface falls
	under, as: a. An amount or a quantity produced that is		behind the transferring of data into the transmit data
	less than what has been		path 400 by the transmit
	estimated. b. The difference		DMA logic The
	between this amount or		underrun detector
	quantity and what has been		determines that a transmit
	estimated.		write TXWR signal is not
			present during an expected
	<u>INTRINSIC EVIDENCE</u> :		interval of the frame
	Claims: see, e.g., claim 15		transmission, then a bad
	("an underrun condition in		frame signal is generated
	which the host interface		line 409 ")
	means in transferring data to		
	the buffer memory falls		EXPERT TESTIMONY:
	behind the network interface		D 1/12
	means in transferring data to		Realtek's expert, Dr. Izhal
	the transceiver"); claim 25		Rubin, may provide
	("a condition in which the		testimony as to the

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporti
	evidence	evidence	evidence
	data transfer circuitry falls		definition of the disputed
	behind the medium access		terms as would be
	controller"); see also claim		understood by one of
	1; claim 18; Specification:		ordinary skill in the releva
	fig. 18; col. 28:48-29:2		art and may provide an
	("According to the present		explanation of the
	invention, this transmit data		technology.
	path includes an underrun		
	detector 413 for detecting a		
	condition in which the		
	transferring of data into the		
	transmit data buffer, or		
	immediate data to the		
	transmit descriptor buffer,		
	by the host interface falls		
	behind the transferring of		
	data into the transmit data		
	path 400 by the transmit		
	DMA logic. The underrun		
	detector 413 is controlled by		
	the transmit control logic		
	411. The transmit control		
	logic 411 indicates intervals		
	across line 414 on line 402.		
	The underrun detector		
	determines that a transmit		
	write TXWR signal in not		
	present during an expected		
	interval of the frame		
	transmission, then a bad		
	frame signal is generated on		
	line 409. In response to the		
	bad frame signal, the CRC		
	data is inverted by the		
	exclusive OR gate 407		
	which causes a bad CRC to		
	be generated for the already		
	transmitted portions of the		
	frame suffering the		
	underrun. Transmit control		
	logic 411 also responds to		
	the bad frame signal on line		
	409 to select the bad CRC		
	data through multiplexer		
	410. Finally, the bad frame		
	signal on line 409 in used		
	for posting status		
	information through the		
	xmitFailureRegister of an		
	underrun condition."); see		
	also Prosecution History:		
	Office Action, Oct. 26,		
	1993, p. 3; Response to		

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence Office Action, Oct. 5, 1994,	evidence	evidence
	p. 2.		
	p. 2.		
	EXTRINSIC EVIDENCE:		
	3Com's expert, Dr. Michael		
	Mitzenmacher may provide		
	an expert report or other		
	form of testimony regarding the technology to which this		
	term relates and how a		
	person having ordinary skill		
	in the art in the field of		
	networking technology		
	would understand this term.		
	3Com reserves the right to		
	rely on testimony by any expert in this action.		
	expert in this action.		
	See also U.S. Patent Nos.		
	5,434,872; 5,732,094;		
	6,327,625; 6,526,446; and		
	6,570,884 (in particular, dependent claims 4 and 6 of		
	the '094); Joint Claim		
	Construction Statement in		
	Cv-05-00098 (VRW).		
	3Com reserves the right to rely on any statement made		
	by any party under the		
	Patent Local Rules.		
"underrun control	PROPOSED CONSTRUCTION:	See proposed construction	Please refer to the
logic"	Logic that detects	pursuant to 35 U.S.C. § 112	construction under 35 U.S.
C 1 in -1-i	underruns.	¶ 6 in Section B.	§ 112 $\P$ 6. To the extent the
found in claim numbers:	DICTIONARY/TREATISE		term requires construction, Realtek asserts that "logic"
numbers.	DEFINITIONS:		should be construed as
'872 patent: 1	See "underrun" in this		"means" and, therefore, this
_	subsection and "logic" in		claim element should be
	subsection 1.		governed by 35 U.S.C. § 11
	INTERPLICIO EMPENOE:		¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6
	INTRINSIC EVIDENCE: Claims: see, e.g., claim 15		does not apply, "underrun
	("an underrun condition in		control logic" should be
	which the host interface		construed as "device for
	means in transferring data to		controlling underrun."
	the buffer memory falls		
	behind the network interface		DICTIONARY/TREATISE
	means in transferring data to the transceiver"); claim 25		<u>DEFINITIONS</u> :
	("a condition in which the		Synopsis, Inc., Electronic
	data transfer circuitry falls		Design Automation
	behind the medium access		Glossary of Terms

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
3		controller, and supplies a bad frame signal to the		The sequence of functions performed by hardware or
3		network"); see also claim 1;		software. Hardware logic is
4		claim 26; Specification:		made up of circuits that
"		see, e.g., fig. 18; col. 28:25-		perform an operation.
5		27; see also Prosecution		Software logic is the
		<u>History</u> : Office Action, Oct.		sequence of instructions in a
6		26, 1993, p. 3; Response to		program.
		Office Action, Oct. 5, 1994,		
7		p. 2.		Newton's Telecom Dictionary:
8		EXTRINSIC EVIDENCE:		"Logica system that
$\mathbb{I}$		3Com's expert, Dr. Michael		could be applied to the
9		Mitzenmacher may provide		relationships between
		an expert report or other form of testimony regarding		propositions to which only a
10		the technology to which this		binary choice of truth
_,		term relates and how a		existed, i.e., yes or no."
11		person having ordinary skill		IBM Dictionary of
12		in the art in the field of		Computing (10th ed. 1993):
14		networking technology would understand this term.		The systematized
13		3Com reserves the right to		interconnection of digital
-		rely on testimony by any		switching functions,
14		expert in this action.		circuits, or devices.
				EXPERT TESTIMONY:
15		See also U.S. Patent Nos. 5,434,872; 5,732,094;		
16		6,327,625; 6,526,446; and		Realtek's expert, Dr. Izhak
10		6,570,884 (in particular,		Rubin, may provide
17		dependent claims 4 and 6 of		testimony as to the definition of the disputed terms as
		the '094); Joint Claim		would be understood by one
18		Construction Statement in Cv-05-00098 (VRW).		of ordinary skill in the
4.0		CV-03-00098 (VKW).		relevant art and may provide
19		3Com reserves the right to		an explanation of the
20		rely on any statement made		technology.
20		by any party under the		
21	((L - 1 C 122	Patent Local Rules.	Proposite solverny servery	Proposite dovatevostica
	"bad frame signal"	PROPOSED CONSTRUCTION: A signal that a frame is bad.	PROPOSED CONSTRUCTION: A specific signal flag	PROPOSED CONSTRUCTION:: a signal indicating that a
22	found in claim	71 Signar that a frame is out.	indicating that a	frame is bad.
	numbers:	DICTIONARY/TREATISE	corresponding frame	
23		DEFINITIONS:	contains invalid data.	DICTIONARY/TREATISE
24	'872 patent: 1	See "frame(s)" in		DEFINITIONS:
	also presented for	subsection 1 for definitions of that term and "indication"		signal
25	construction in:	signal" in subsection 1 for		Newton's' Telecom
		definitions of "signal."		Dictionary (fourth edition,
26	'094 patent: 21	bad: The American Heritage		<u>1991)</u>
		Dictionary of the English		Signal: 1. An electrical
27		Language (4th ed. 2000): adj. 1. Not achieving an		wave used to convey information 2. An alert. 3.
28		auj. 1. 110t acmeving an	<u> </u>	miorination 2. All alert. 3.
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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	adequate standard; poor: a		An acoustic device (e.g. a
	bad concert 8. Injurious		bell) or a visual device (e.g
	in effect; detrimental: bad		a lamp) which calls
	habits. 9. Not working		attention. To transmit an
	properly; defective: a bad		information signal or
	telephone connection. 10.		alerting signal.
	Full of or exhibiting faults		
	or errors: bad grammar.		McGraw Hill Electronics
			Dictionary (fifth edition,
	INTRINSIC EVIDENCE:		<u>1994)</u>
	Claims: see, e.g., claim 4		Signal: Any variation in ar
	("the bad frame signal		electrical current, visible o
	comprises a corrupted error		nonvisible light, audible or
	detection code"); see also		ultrasonic energy that
	claim 1; claim 15; claim 16;		conveys information.
	claim 18; claim 20; claim		Signals can be coded in
	25; claim 26; Specification:		frequency, phase, or
	see, e.g., fig. 18; col. 19:35-		amplitude to separate them
	38; col. 28:38-40; col.		from unwanted noise.
	28:48-29:2; Fig. 18; col.		
	28:58-29:2; 29:40-44; <u>see</u>		<u>bad</u> :
	also Prosecution History:		
	Office Action, Oct. 26,		The American Heritage
	1993, p. 3; Office Action,		Dictionary of the English
	Oct. 26, 1993, p. 6;		Language (4th Ed. 2000):
	Response to Office Action,		adj. 1. Not achieving an
	Oct. 5, 1994, p. 2; Response		adequate standard; poor: a
	to Office Action, Oct. 5,		bad concert 8. Injuriou
	1994, p. 3.		in effect; detrimental: bad
			habits. 9. Not working
	EXTRINSIC EVIDENCE:		properly; defective: a bad
	3Com's expert, Dr. Michael		telephone connection. 10.
	Mitzenmacher may provide		Full of or exhibiting faults
	an expert report or other		or errors: bad grammar.
	form of testimony regarding		
	the technology to which this		
	term relates and how a		Intrinsic Evidence:
	person having ordinary skill		
	in the art in the field of		'872 patent at 28:48-29:2;
	networking technology		'094 patent at 27: 15-35
	would understand this term.		("According to the present
	3Com reserves the right to		invention, this transmit dat
	rely on testimony by any		path includes an underrun
	expert in this action.		detector 413 for detecting
	G 1 170 5		condition in which the
	See also U.S. Patent Nos.		transferring of data into th
	5,434,872; 5,732,094;		transmit data buffer,, l
	6,327,625; 6,526,446; and		the host interface falls
	6,570,884; Joint Claim		behind the transferring of
	Construction Statement in		data into the transmit data
	Cv-05-00098 (VRW).		path 400 by the transmit
			DMA logic The
	3Com reserves the right to		underrun detector

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
	rely on any statement made by any party under the Patent Local Rules.		determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated
			line 409")  '872 patent, Fig. 18; '094 patent, Fig. 18 ("a signal line identified as "bad
			frame" and connected "to host interface.")
			EXPERT TESTIMONY:
			Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definiti
			of the disputed terms as would be understood by or of ordinary skill in the
			relevant art and may provi an explanation of the technology.
"buffer" found in claim	PROPOSED CONSTRUCTION: A memory for temporary storage of data.	PROPOSED CONSTRUCTION: Term is used only in phrase "buffer memory." See	Same as " <b>buffer memory</b> identified above.
numbers: '872 patent: 1, 10, 21	DICTIONARY/TREATISE DEFINITIONS: See "buffer"	construction of "buffer memory."	
also presented for	in subsection 1.		
construction in: '459 patent: 1	INTRINSIC EVIDENCE: Claims: see, e.g., claim 2 ("the transmit buffer		
'094 patent: 1, 9, 21, 28, 39, 47	includes a transmit descriptor ring and a transmit data buffer");		
	claim 7 ("The apparatus of claim 1, wherein the buffer includes a transmit		
	descriptor ring buffer and a transmit data buffer, and the		
	means for transferring includes: transmit descriptor logic for mapping transmit		
	descriptors from the system to the transmit descriptor		
	ring buffer; and download logic, responsive to the transmit descriptors in the		

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(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	
	11 0	construction and supporting	construction and supporting
	evidence	evidence	evidence
	buffer, for retrieving data		
	from memory in the system		
	and storing retrieved data in		
	the transmit data buffer.");		
	see also claim 1; claim 3;		
	claim 9; claim 10; claim 11;		
	claim 15; claim 18; claim		
	21; claim 22; Specification:		
	see, e.g., figs. 2, 6-10E; col		
	1:47-54 ("Transmit data		
	buffers are to be		
	distinguished from first-in-		
	first-out FIFO systems, in		
	which the sending system		
	downloads data of a frame		
	into the FIFO, while the		
	network adapter unloads the		
	FIFO during a transmission.		
	The data in FIFOs cannot be		
	retained and reused by the		
	media access control		
	functions, or by the host,		
	like data in transmit data		
	buffers."); col. 1:65-67		
	("Furthermore, the prior art		
	systems which use transmit		
	data buffers require the host		
	or sending system to		
	manage the transmit data		
	buffer."); col. 2:13-18 ("The		
	present invention provides		
	for the early initiation of		
	transmission of data in a		
	network interface that		
	includes a dedicated		
	transmit buffer."); col. 2:35-		
	37 ("the transmit data buffer		
	includes a transmit		
	descriptor ring, and a		
	transmit data buffer"); col.		
	13:12-27 ("In the preferred		
	system, the adapter uses		
	32K bytes of static RAM for		
	the transmit buffers, receive		
	buffers, control structures,		
	and various status and		
	statistics registers. Several		
	of the regions in the		
	adapter's memory defined		
	in Fig. 5 provide defined		
	data structures. A. Transmit		
	Data Buffer The transmit		
	data buffer occupies 3K		

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	T	T	T	T
1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
_	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
_		bytes as mentioned above.		
3		This region is divided into		
		two 1.5K buffers. Only the		
4		data that are downloaded to		
_		the adapter via bus master		
5		transfers are stored in these buffers. The controller will		
		use both the contents of the		
6		transmit data buffer and the		
_		immediate data portion of		
		the transmit descriptors,		
		when encapsulating a frame		
8		for transmission. The		
		adapter automatically		
9		alternates the use of the		
10		buffers after choosing the		
10		buffer closest to the base of		
11		the memory as the power up		
11		default."); see also col.		
12		1:36-2:10; col. 2:14-27; col.		
12		2:44-48; col. 3:21-27; col. 3:59-65; col. 4:29-33; col.		
13		4:38-45; col. 4:64-5:22; col.		
		5:41-43; col. 5:57-61; col.		
14		6:33-35; col. 8:57-64; col.		
		9:1-3; col. 9:8-11; col. 9:13-		
15		16; col. 9:19-22; col. 9:29-		
		32; col. 9:37-39; col. 9:62-		
16		65; col. 9:68-10:7; col.		
		10:16-18; col. 10:20-23; col.		
17		11:17-20; col. 11:22-25; col. 11:33-39; col. 11:59-61; col.		
1.0		12:4-6; col. 12:43-46; col.		
18		12:58-68; col. 13:2-8; col.		
10		13:12-15; col. 13:17-48; col.		
19		13:52-54; col. 13:61-66; col.		
20		14:17-20; col. 15:25-46; col.		
20		15:58-60; col. 16:1-7; col.		
21		16:9-12; col. 16:28-32; col.		
		16:35-39; col. 16:52-56; col.		
22		16:67-17:3; col. 17:7-22; col. 17:24-31; col. 17:33-34;		
		col. 17:54-56; col. 17:65-68;		
23		col. 18:21-25; col. 18:44-46;		
		col. 18:49-52; col. 19:45-47;		
24		col. 21:22-26; col. 21:42-45;		
ا ۽ ۽		col. 22:60-62; col. 22:1-2;		
25		col. 22:4-8; col. 22:20-23;		
26		col. 22:27-32; col. 22:44-51;		
26		col. 22:53-56; col. 22:67- 23:4; col. 23:43-45; col.		
27		23:48-51; col. 23:60-65; col.		
<i>- 1</i>		24:26-27; col. 24:29-32; col.		
20	<u> </u>		1	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	24:37-39; col. 24:39-40; col.		
	24:43-52; col. 25:48-50; col.		
	28:48-54; col. 29:5-9; col.		
	29:25-31; <u>see also</u>		
	Prosecution History: Office		
	Action, Oct. 26, 1993, p. 2;		
	Office Action, Oct. 26,		
	1993, p. 3; Office Action,		
	Oct. 26, 1993, p. 4; Office		
	Action, Oct. 26, 1993, p. 5;		
	Office Action, Oct. 26,		
	1993, p. 6; Part 131		
	Affidavit, p. 1; Part 131		
	Affidavit, p. 2; Part 131		
	Affidavit, p. 3; Part 131		
	Affidavit, p. Ex. 1, p. 6; Response to Office Action,		
	Feb. 23, 1994, p. 2;		
	Response to Office Action,		
	Feb. 23, 1994, pp. 4-5;		
	Response to Office Action,		
	Feb. 23, 1994, p. 5;		
	Response to Office Action,		
	Feb. 23, 1994, p. 6; Office		
	Action, Jul. 6, 1994, p. 2;		
	Response to Office Action,		
	Oct. 5, 1994, p. 2; Response		
	to Office Action, Oct. 5,		
	1994, p. 3.		
	, p. 5.		
	EXTRINSIC EVIDENCE:		
	3Com's expert, Dr. Michael		
	Mitzenmacher may provide		
	an expert report or other		
	form of testimony regarding		
	the technology to which this		
	term relates and how a		
	person having ordinary skill		
	in the art in the field of		
	networking technology		
	would understand this term.		
	3Com reserves the right to		
	rely on testimony by any		
	expert in this action.		
	See also section I.A, supra		
	(agreed upon definition for		
	"buffer" in '625 and '884		
	patents); U.S. Patent Nos.		
	5,434,872; 5,732,094;		
	6,327,625; 6,526,446; and		
	6,570,884; Joint Claim		
	Construction Statement in		

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
2		Cv-05-00098 (VRW).		
3		3Com reserves the right to		
4		rely on any statement made		
_		by any party under the Patent Local Rules.		
5	"buffer memory"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	Same as "buffer memory"
6		A memory for temporary	Dedicated random access	identified above.
	found in claim numbers:	storage of data.	memory that (1) stores	
7	numbers.	DICTIONARY/TREATISE	transmit data, (2) is distinct from a FIFO, (3) can always	
8	'872 patent: 1, 10, 21	DEFINITIONS:	retransmit a frame of data	
٥		See "buffer" and	without having to retrieve it	
9	also presented for	"memory" in subsection 1.	from a host, and (4) is	
	construction in:	INTRINSIC EVIDENCE:	controlled independently of the host system.	
10	'459 patent: 1	Claims: see, e.g., claim 2	and most system.	
, ,	•	(depending from claims 1	REFERENCES:	
11	'094 patent: 1, 9, 21,	and including a limitation	D. mari ya Camaran a mari a	
12	28, 39, 47	that "the transmit buffer includes a transmit	PATENT SPECIFICATION: Claim 2 of the '872 patent	
		descriptor ring and a	recites "The apparatus of	
13		transmit data buffer"); see	claim 1, wherein the	
		also claim 1; claim 3;	transmit buffer includes"	
14		claim7; claim 10; claim 11;	(emphasis added).	
15		claim 15; claim 18; claim 21; claim 22; Specification:	Claim 7 of the '872 patent	
		see, e.g., col. 2:35-37 ("the	recites "The apparatus of	
16		transmit data buffer includes	claim 1, wherein the buffer	
		a transmit descriptor ring,	includes a transmit	
17		and a transmit data buffer"); see also col. 1:14-16; col.	descriptor ring buffer and a transmit data buffer"	
18		2:13-17; col. 1:36-2:6; col.	(emphasis added).	
0		3:59-65; col. 5:57-61; col.	( 1 )	
9		13:18-48; col. 13:59-68; <u>see</u>	"Early initiation of	
		also Prosecution History: Office Action, Oct. 26,	transmission of data in a network interface that	
20		1993, p. 2; Office Action,	includes a dedicated	
, 1		Oct. 26, 1993, p. 2; Office	transmit buffer is provided	
21		Action, Oct. 26, 1993, p. 3;	in a system which includes	
22		Part 131 Affidavit, p. 1; Part 131 Affidavit, p. 2;	logic for transferring frames	
		Response to Office Action,	of data composed by the host computer into the	
23		Feb. 23, 1994, p. 2;	transmit buffer." ('872	
ا ر		Response to Office Action,	Abstract and '094 Abstract) <sup>2</sup>	
24		Oct. 5, 1994, p. 2.	(emphasis added).	
25		EXTRINSIC EVIDENCE:	"The present invention	
		3Com's expert, Dr. Michael	The present invention	
26		<u> </u>	•	1

<sup>&</sup>lt;sup>2</sup> Citations to the description of the '872 patent can also be found in the description of the related '094 patent; all citations to the '872 patent apply equally to the '094 patent.

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
	Mitzenmacher may provide	provides for the early	evidence
	an expert report or other	initiation of transmission of	
	form of testimony regarding	data in a network interface	
	the technology to which this	that includes a <i>dedicated</i>	
	term relates and how a person having ordinary skill	transmit buffer. The system includes logic for	
	in the art in the field of	transferring frames of data	
	networking technology	composed by the host	
	would understand this term.	computer into the transmit	
	3Com reserves the right to	buffer." ('872; Col. 2: 13-	
	rely on testimony by any expert in this action.	17) ( <i>See also</i> '872; Col. 1: 14-16) (emphasis added).	
	expert in this action.	14-10) (chiphasis added).	
	See also section I.A, supra	"According to another	
	(agreed upon definition for	aspect of the present	
	"buffer" in '625 and '884 patents); U.S. Patent Nos.	invention, the <i>transmit</i> buffer includes a transmit	
	5,434,872; 5,732,094;	descriptor ring, and a	
	6,327,625; 6,526,446; and	transmit data buffer. The	
	6,570,884; Joint Claim	host system composes a	
	Construction Statement in Cv-05-00098 (VRW).	frame by storing a transmit	
	CV-03-00038 (VKW).	descriptor in the adapter managed transmit descriptor	
		ring." ('872; Col. 2: 35-39)	
		(emphasis added).	
		"Some network adapter	
		interfaces include dedicated	
		transmit buffers into which	
		a frame of data composed	
		by the sending system can be downloaded by the	
		sending system. The frame	
		is then stored in the <i>transmit</i>	
		data buffer until the media	
		access control functions associated with transmitting	
		the frame on the network	
		have successfully	
		transmitted the frame, or	
		cancelled the frame transmission. If the frame	
		transmission is cancelled,	
		the data may be retained in	
		the transmit data buffer	
		until the sending system	
		initiates a second attempt to transmit the frame.	
		Transmit data buffers are to	
		be distinguished from first-	
		in-first-out FIFO systems, in	
		which the sending system downloads data of a frame	
		downloads data of a frame	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		into the FIFO, while the	
		network adapter unloads the	
		FIFO during a transmission.	
		The data in FIFOs cannot be	
		retained and reused by the	
		media access control	
		functions, or by the host,	
		like data in <i>transmit data</i>	
		buffers." ('872; Col. 1: 36-	
		54) (emphasis added).	
		"Although transmit data	
		buffers enable a sending	
		system to compose and	
		download a frame into the	
		transmit data buffer, and	
		then attend to other tasks	
		while the network adapter attempts to transmit the	
		frame, it suffers the	
		disadvantage that	
		transmission of a frame is	
		delayed until the entire	
		frame has been downloaded	
		into the buffer. Thus,	
		transmit data buffer type	
		systems improve host	
		system efficiency at the expense of network	
		throughput." ('872; Col. 1:	
		55-63) (emphasis added).	
		"Furthermore, the prior art	
		systems which use transmit	
		data buffers require the host	
		or sending system to	
		manage the transmit data	
		buffer. A network interface	
		controller transfers data	
		from the host managed	
		transmit data buffer using	
		DMA techniques through a	
		FIFO buffer in the interface	
		controller and on to the	
		network." ('872; Col. 1: 65	
		- Col. 2: 2) (emphasis	
		added).	
		"Donragantations and	
		"Representative prior art	
		systems include the	
		National Semiconductor DP83932B, a systems-	
		oriented network interface	
	İ	i onenied network interface	Ī

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		controller (SONIC) and the Intel 82586 local area	
		network coprocessor."	
		('872; Col. 2: 3-6).	
		(872, Col. 2. 3-0).	
		"The transmit data buffer	
		occupies 3K bytes as	
		mentioned above. This	
		region is divided into two	
		1.5K buffers. Only the data	
		that are downloaded to the	
		adapter via bus master	
		transfers are stored in these	
		buffers. The controller will	
		use both the contents of the	
		transmit data buffer and the	
		immediate data portion of	
		the transmit descriptors,	
		when encapsulating a frame	
		for transmission. The	
		adapter automatically alternates the use of the	
		buffers after choosing the	
		buffer closest to the base of	
		the memory as the power up	
		default." ('872; Col. 13: 18-	
		27) (emphasis added).	
		"The <i>transmit buffers</i> are	
		shared by the download	
		DMA logic and the transmit	
		DMA logic. The transmit	
		DMA logic may switch	
		from buffer 0 to buffer 1	
		and back again freely. The	
		only restriction being the	
		availability of transmit data	
		as defined by the transmit start threshold register. The	
		transmit DMA module	
		switches from one buffer to	
		the other whenever it has	
		completed a transmission.	
		The buffer switch occurs	
		regardless of whether or not	
		the transmission was	
		successful and regardless of	
		whether or not bus master	
		download data were used in	
		the preceding transmission."	
		('872; Col. 13: 28-38)	
		(emphasis added).	
		Í	i

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		"The download DMA	
		module may only switch	
		from one <i>buffer</i> to the other,	
		if the <i>buffer</i> it is going to	
		switch to is not being used	
		by the transmit DMA	
		module. Download DMA	
		will attempt to switch from	
		one <i>buffer</i> to another every	
		time it completes processing	
		of a transmit descriptor as	
		described below, regardless	
		of whether or not any bus	
		master operations were	
		called for in the preceding	
		descriptor. However, it will	
		not change to a <i>buffer</i> that is	
		in use by the transmit DMA	
		module." ('872; Col. 13:	
		39-48) (emphasis added).	
		(T)	
		"The transmit data buffer	
		occupies 3K bytes as	
		mentioned above. This	
		region is divided into two	
		1.5K buffers. Only the data	
		that are downloaded to the	
		adapter via bus master transfers are stored in these	
		buffers. The controller will	
		use both the contents of the	
		transmit data buffer and the	
		immediate data portion of	
		the transmit descriptors,	
		when encapsulating a frame	
		for transmission. The	
		adapter automatically	
		alternates the use of the	
		buffers after choosing the	
		buffer closest to the base of	
		the memory as the power up	
		default." ('459; Col. 13: 59-	
		68) (emphasis added).	
		, ( 1 2 22.2).	
		PROSECUTION HISTORY:	
		The following citation to	
		the prosecution history of	
		the '872 patent supports D-	
		Link's proposed claim	
		construction	
	1	1	1

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supportin
	evidence	application that issued as the	evidence
		'872 patent, in a Response	
		dated February 23, 1994,	
		3Com stated the following:	
		"Accordingly, the	
		Firoozmand, et al. reference	
		does not initiate	
		transmission to the network	
		upon the threshold	
		determination. Rather,	
		transmission to the network	
		is initiated only when there is a full frame available in	
		the buffer. When the token	
		has been received by the	
		transmitting station, and it	
		has a full frame for	
		transmission, then a	
		transmission process is	
		begun. The transmission	
		process continues, relying	
		on the threshold	
		determination to keep the	
		pipeline full, only while the	
		token is held by the	
		transmitting station."	
		"The environment is	
		substantially different from	
		the CSMA/CD network,	
		which begins transmission to the medium access	
		controller as soon as the	
		threshold determination is	
		met for an incoming frame.	
		The MAC may succeed in	
		transmitting the frame, may	
		suffer collisions, or may	
		suffer other types of errors	
		which require backoff.	
		Thus, the adapter as claimed	
		in new claims 24-29,	
		initiates transmission	
		without being assured that	
		the medium access	
		controller is able to gain	
		access to the communications medium.	
		This is a much more	
		sophisticated control	
		environment than that	
		required by the FDDI	
	1	system of Firoozmand, et	1

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
		al." Response dated February 23, 1994, p. 5.	
		EXTRINSIC EVIDENCE:	
		PRIOR ART:	
		Datesheet for "82596CA High-Performance 32-Bit	
		Local Area Network Coprocessor," November	
		1989, Intel Corp (Disclosed in D-Link's Preliminary	
		Infringement Contentions), pg. 2: "Two large,	
		independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate	
		long bus latencies and provide programmable	
		thresholds that allow the user to optimize bus	
		overhead for any worst-case bus latency."	
		Datasheet for "The SUPERNET 2 Family for	
		FDDI", October 1991, Advanced Micro Devices,	
		Inc. (Disclosed in D-Link's Preliminary Infringement	
		Contentions), pg. 2-37: "The transmit FIFO (Figure	
		1) is a 36-bit by 9-word first-in-first-out register that	
		temporarily stores data to be transmitted. In this way, continuity of data	
		transmission is assured by providing a way to store a	
		portion of the output data stream to compensate for	
		delays involved in accessing the buffer memory."	
		1992 Local Area Network	
		Databook Including Datasheet For DP83932B Systems-Oriented Network	
		Interface Controller (SONIC), 1992, National	
		Semiconductor Corp, pg.1-	

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1	Claim language	2Com's nuonosad	D. Link's proposed	Pagltak's proposed
1	Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
2	,	evidence	evidence	evidence
3			295: "The SONIC incorporates two	
			independent 32-byte FIFOs	
4			for transferring data to/from	
5			the system interface and from/to the network. The	
			FIFOs, providing temporary	
6			storage of data, free the host system from the real-time	
7			demands on the network."	
			DICTIONARY/TREATISE	
8			DEFINITIONS:	
9			McGraw-Hill Illustrated	
10			Telecom Dictionary, Fourth	
10			Edition, 2001, pg. 83: Buffer - "A temporary	
11			storage (memory) device for	
12			data. A buffer is basically a box with RAM inside it. A	
12			common application for	
13			buffers is to collect a stream	
14			of data and temporarily store it until another device,	
			such as a PC or server asks	
15			the buffer to download it. This is useful when the PC,	
16			server or LAN could be out	
1.7			of service for a period of time. When the server or	
17			PC is returned to service it	
18			just asks for the data from the buffer and it is	
10			downloaded. The buffer is	
19			then empty and ready to receive more data."	
20			receive more data.	
21			EXPERT TESTIMONY:	
22			D-Link's expert, Howard	
22			Frazier, may provide testimony as to the	
23			definition of the disputed	
24			terms as would be	
			understood by one of ordinary skill in the relevant	
25			art and may provide an	
26			explanation of the technology.	
27			D-Link also incorporates by reference Realtek's	
28		<u> </u>	1 reference realter 5	

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence references.	Realtek's proposed construction and supporting evidence
"host system"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
found in claim numbers:	A computer that communicates over a network	Any system or computer that communicates over a network	Any system or computer that communicates over a network
'872 patent: 1, 10, 21	<u>DICTIONARY/TREATISE</u> DEFINITIONS: Webster's New	INTRINSIC EVIDENCE	Evidence
also presented for construction in:	World Computer Dictionary (10th ed. 2003): 1. In the	(872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62)	(872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62)
'459 patent: 1	Internet, any computer that can function as the	Furthermore, the prior art systems which use transmit	Furthermore, the prior art systems which use transmit
'094 patent: 1, 9, 21, 28, 39, 47	beginning and end point of data transfers. An Internet host has a unique Internet	data buffers require the <i>host</i> or sending system to manage the transmit data	data buffers require the hos or sending system to manage the transmit data
'884 patent: 1	address (called an IP address) and a unique	buffer.	buffer.
	domain name. 2. In networks and	(872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns.	(872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns.
	telecommunications generally, a server that	59-64) As shown in FIG. 1, such system for	59-64) As shown in FIG. 1 such system for
	performs centralized functions, such as making	communicating data includes a host data	communicating data includes a host data
	program or data files available to other	processing system, generally referred to by	processing system, generally referred to by
	computers; The American Heritage Dictionary of the	reference number 1, which includes a host system bus	reference number 1, which includes a host system bus
	English Language (4th ed. 2000): Computer Science. A	2, a host central processing unit 3, host memory 4, and	2, a host central processing unit 3, host memory 4, and
	computer containing data or programs that another	other host devices 5, all communicating across the	other host devices 5, all communicating across the
	computer can access by means of a network or	bus 2	bus 2
	modem; Dictionary of Computing (3d ed. 1990):		(884: Col. 2, lns. 39-44)
	Host computer (host): A computer that is attached to		The invention is particular suited to environments in
	a network and provides services other than simply		which the host system is actively handling
	acting as a store-and- forward processor or		communications and other processing tasks, and in
	communication switch.		which the adapter is able to take over some specialized
	INTRINSIC EVIDENCE: Claims claim 1; ; claim 10; ;		tasks without interfering with the active processing
	claim 15; claim 18; ; claim 21; Specification: see, e.g.,		the host system.
	figs. 1-3; col.4:7-11 ("The network adapter 6 is, in		
	turn, connected to an adapter memory 9, which is		

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	managed by the interface		
	controller 6 or by the host		
	CPU3"); <u>see also</u> col. 1; col.		
	1:51-55; col. 1:61-63; col.		
	1:65-67; col. 1-2:67-3; col.		
	2:16-18; col. 2:18-22; col.		
	2:27-31; col. 2:31-35; col.		
	2:37-39; col. 2:55-62; col.		
	3:44- 4:7; col. 3:11-14; col.		
	3:14-17; col. 3:17-19; col. 3:		
	59-4:2; col. 4:2-3; col. 4:11-		
	13; col. 4:13-16; col. 4:19-		
	21; col. 4:26-29; col. 4:29-		
	30; col. 4:30-33; col. 4:33-		
	34; col.4: 46-47; col.4: 47-		
	50; col. 4:56-58; col. 4:58-		
	61; col.4:61-62; col.4:62-64;		
	col.4:64-67; col. 5:5-14; col.		
	5:14-20; col. 5:20-23; col.		
	5:28-31; col. 5:31-33; col.		
	5:33-36; col. 5:50-53; col.		
	5:57-60; col. 5:62-64;		
	col.6:26-28; col.6:33-35;		
	col.6:48-51; col.7:18-22;		
	col.7:60-64; col.7:64-66;		
	col. 8:5-7; col. 8:9-14; col.		
	8:28-29; col. 8:44-47; col.		
	8:55-57; col. 8:64-1; col. 9-		
	10:68-4; col. 10:4-11; col.		
	10:14-16; col. 10:23-27; col.		
	10:27-31; col. 10:31-35; col. 10:35-38; col. 10:4-45; col.		
	10:60-63; col. 11:43-47; col.		
	11:47-49; col. 11:49-51; col.		
	11:51-53; col. 11:53-54; col. 11:54-57; col. 11:64-68; col.		
	11-12:68-4; col. 12:4-7; col.		
	12:15-17; col. 12:17-23; col.		
	12:23-24; col. 12:24-28; col.		
	12:33-37; col. 12:37-39; col.		
	12:39-41; col. 12:41-43; col.		
	12:49-50; col. 12:58-61; col.		
	12:61-65; col. 12:65-1; col.		
	13:1-2; col. 13:58-61; col.		
	13-14:67-4; col.14:4-6;		
	col.14:30-33; col.14:36-38;		
	col.14:49-53; col.14:56-58;		
	col.14:62-65; col.14:65-68;		
	col. 14-15:68-3; col.15:10-		
	13; col.15:19-20; col.15:20-		
	25; col.15:25-27; col.15:27-		
	29; col.15:29-32; col.15:35-		
	27, 001.13.29-32, 001.13.33-		1

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
1	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2	\ 1 /	evidence	evidence	evidence
_		44; col.15:46-48; col.15:58-		
3		61; col.15:61-64; col.16:1-3;		
_ ,		col.16:5-6; col.16:9-12;		
4		col.16:12-14; col.16:14-22; col.16:24-27; col.16:28-32;		
5		col.16:32-34; col.16:35-40;		
3		col.16:52-56; col.16:56-58;		
6		col.16:58-61; col.16:61-63;		
		col.16:63-67; col. 16-17:67-		
7		3; col. 17:14-19; col. 17:33-		
_		38; col. 17:38-40; col. 17:40-46; col. 17:50-53; col.		
8		17:56-59; col. 18:1-3; col.		
9		18:6-10; col. 18:18-21; col.		
9		18:21-25; col. 18:41-44; col.		
10		18:47-49; col. 18:53-57; col.		
		19:3-5; col. 19:50-55; col. 20:14-17; col. 20:39-42; col.		
11		20:63-66; col. 21:1-3; col.		
		21:7-11; col. 21:22-26; col.		
12		21:49-51; col. 21:51-54; col.		
1.2		22:63-66; col. 22:66-1; col.		
13		22:1-4; col. 22:12-15; col.		
14		22:15-16; col. 22:27-33; col. 22:33-34; col. 22:34-38; col.		
17		22:38-39; col. 22:60-63; col.		
15		22:63-65; col. 23:12-13; col.		
		24:47-52; col. 25:27-31; col.		
16		25:48-51; col. 25:52-60; col.		
1.7		26:9-10; col. 26:65-1; col. 27:33-35; col. 28:48-54; col.		
17		29:39-40; col. 29:46-48; col.		
18		29:48-51; see also		
10		<u>Prosecution History</u> : Office		
19		Action, Oct. 26, 1993, p. 2;		
		Office Action, Oct. 26, 1993, p. 3; Office Action,		
20		Oct. 26, 1993, p. 5; Part 131		
		Affidavit, p. 2; Part 131		
21		Affidavit, p. 2; Part 131		
22		Affidavit, p. 2; Part 131		
		Affidavit, p. Ex. 1, p. 11;		
23		Part 131 Affidavit, p. Ex. 1, p. 11; Response to Office		
_		Action, Feb. 23, 1994, p. 2;		
24		Office Action, Jul. 6, 1994,		
		p. 2; Office Action, Jul. 6,		
25		1994, p. 2; Response to		
26		Office Action, Oct. 5, 1994,		
26		p. 2.		
27		EXTRINSIC EVIDENCE:		
- '		3Com's expert, Dr. Michael		
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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
(aisputea terms in <b>bota</b> )	evidence	evidence	evidence
	Mitzenmacher may provide		
	an expert report or other form of testimony regarding		
	the technology to which this		
	term relates and how a		
	person having ordinary skill in the art in the field of		
	networking technology		
	would understand this term.		
	3Com reserves the right to		
	rely on testimony by any expert in this action.		
	expert in this detroit.		
	See also U.S. Patent Nos.		
	5,434,872; 5,732,094; 6,327,625; 6,526,446; and		
	6,570,884; Joint Claim		
	Construction Statement in		
	Cv-05-00098 (VRW).		
	3Com reserves the right to		
	rely on any statement made		
	by any party under the Patent Local Rules.		
"logic"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	Please refer to the
_	Circuitry and/or		construction under 35
found in claim numbers:	programming	When used as a standalone term in the claims, "logic" is	U.S.C. § 112 ¶ 6 for the separate claim limitations of
numbers.	DICTIONARY/TREATISE	an unspecified claim	the identified claims. To the
'872 patent: 1, 21	DEFINITIONS: See "logic" in	element defined only by its	extent this term requires
alaa muaaantad fan	subsection 1.	function and thus requires	construction, Realtek asser
also presented for construction in:	INTRINSIC EVIDENCE:	interpretation under invokes 35 U.S.C. § 112 ¶ 6.	that "logic" (or "logic for") as used in the identified
	Claims: claim 1; claim 4;	50 0.5.0. 3 112    0.	claims should be construed
'459 patent: 1	claim 5; claim 7; claim 9;	In computer software or	as "means" (or "means for
'625 patent: 23	claim 11; claim 13; claim 14; claim 15; claim 19;	hardware context, "means" or "means for."	and, therefore, the associated claim elements
023 patent. 23	claim 21; claim 22; claim	or means for.	should be governed by 35
'884 patent: 1	23; claim 25; claim 26;	See discussion in section	U.S.C. § 112 ¶ 6. If the
	Specification: figs. 1, 2, 5, 9, 11-18; col. 2:16-18; col.	below concerning 35 U.S.C. § 112 ¶ 6 constructions for	Court determines that 35 U.S.C. § 112 ¶ 6 does not
	2:22-31; col. 2:48-51; col.	phrases including "logic."	apply, "logic" should be
	3:28-34; col. 3:37-44; col.		construed as "device."
	3:52-54; col. 4:11-16; col. 4:26-45; col. 4:47-49; col.		DICTIONARY/TREATISE
	4:56-58; col. 4:67-5:13; col.		<u>DEFINITIONS</u> :
	6:15-18; col. 7:44-46; col.		
	9:1-3; col. 9:13-16; col.		Synopsis, Inc., Electronic
	10:65-11:2; col. 11:25-31; col. 11:36-39; col. 11:51-61;		Design Automation Glossary of Terms
	col. 11:64-68; col. 12:7-15;		The sequence of functions
	col. 12:17-22; col. 12:37-39;		performed by hardware or
	col. 13:28; col. 13:29-31;		software. Hardware logic is

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		T		,
1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting evidence	construction and supporting
4		evidence col. 16:9-23; col. 16:32-35;	eviaence	evidence made up of circuits that
3		col. 16:40-45; col. 16:52-56;		perform an operation.
		col. 16:67-17:14; col. 17:19-		Software logic is the
4		28; col. 17:47-50; col.		sequence of instructions in a
		17:60-62; col. 21:49-50; col.		program.
5		22:66-68; col. 22:1-4; col.		
		22:12-23; col. 22:26-32; col. 22:43-44; col. 22:48-59; col.		Newton's Telecom
6		23:5-10; col. 23:20-29; col.		<u>Dictionary</u> :
7		24:9-12; col. 24:17-18; col.		"Logica system that
/		24:24-25; col. 24:32-34; col.		could be applied to the relationships between
8		24:39-40; col. 24:48-52; col.		propositions to which only a
		24:55-60; col. 24:67-25:2;		binary choice of truth
9		col. 25:3-7; col. 25:19-21; col. 26:37-39; col. 26:46-49;		existed, i.e., yes or no."
		col. 26:61-62; col. 27:36-38;		
10		col. 28:25-29; col. 28:33-45;		IBM Dictionary of
11		col. 28:48-58; col. 28:65-67;		Computing (10th ed. 1993): The systematized
11		see also Prosecution		interconnection of digital
12		History: Office Action, Oct. 26, 1993, p. 2; Office		switching functions,
12		Action, Oct. 26, 1993, p. 3;		circuits, or devices.
13		Part 131 Affidavit, pp. 2-3;		F
		Response to Office Action,		EXPERT TESTIMONY:
14		Feb. 23, 1994, p. 5;		Realtek's expert, Dr. Izhak
1		Response to Office Action,		Rubin and/or Dr. Nick
15		Oct. 5, 1994, p. 2; Response to Office Action, Oct. 5,		Bambos, may provide
16		1994, p. 3.		testimony as to the
10		, 1		definition of the disputed terms as would be
17		EXTRINSIC EVIDENCE:		understood by one of
		3Com's expert, Dr. Michael		ordinary skill in the relevant
18		Mitzenmacher may provide an expert report or other		art and may provide an
1.0		form of testimony regarding		explanation of the
19		the technology to which this		technology.
20		term relates and how a		
20		person having ordinary skill		
21		in the art in the field of networking technology		
		would understand this term.		
22		3Com reserves the right to		
22		rely on testimony by any		
23		expert in this action.		
24		See also U.S. Patent Nos.		
		5,434,872; 5,732,094;		
25		6,327,625; 6,526,446; and		
		6,570,884; Joint Claim		
26		Construction Statement in		
27		Cv-05-00098 (VRW).		
27		3Com reserves the right to		
28		2 com reserves the right to	1	1

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supportine evidence
	rely on any statement made by any party under the Patent Local Rules.		
"feedback"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION
Toubuch	Information from output	Information derived from an	Information from output
found in claim	returned to the input	output to adjust an input.	that is returned to input
numbers:	1		•
	DICTIONARY/TREATISE		DICTIONARY/TREATISE
'872 patent: 10	<u>DEFINITIONS</u> : <u>Newton's</u>	REFERENCES:	DEFINITIONS:
	Telecom Dictionary (17th		
also presented for	ed. 2001): The return of part	PATENT SPECIFICATION:	Webster's Ninth New
construction in:	of an output signal back to	The following citations	Collegiate Dictionary (nin
	the input side of the device;	support D-Link's proposed	edition, 1988)
'094 patent: 21, 47	The American Heritage	claim construction.	Feedback: 1. the return to
	Dictionary of the English	"The transmit logic 39 also	the input of a part of the
	Language (4th ed. 2000):	supplies status information across line 44 to the host	output of a machine, syste or process (as for producir
	The return of a portion of the output of a process or	interface logic 31, for	changes in an electronic
	system to the input,	posting to the host system.	circuit that improve
	especially when used to	The status information	performance or in an
	maintain performance or to	includes indications of	automatic control device
	control a system or process;	underrun conditions and	that provide self-corrective
	see also Dictionary of	may be used by the host to	action.)
	Computing (1st ed. 1983):	optimize the value in the	detion.)
	Feedback queue: A form of	threshold store 43." ('872;	The American Heritage
	scheduling mechanism often	Col. 4: 56-60) (emphasis	Dictionary of the English
	used in multiaccess systems.	added).	Language (4th ed. 2000)
	Individual processes are	,	The return of a portion of
	allocated a quantum of time	"The value for this register	the output of a process or
	on the processor. A process	may be programmed by the	system to the input,
	once started is allowed to	host to optimize	especially when used to
	run until it has exhausted its	performance. If set too low,	maintain performance or t
	quantum, until it initiates a	system latencies or	control a system or proces
	transfer on a peripheral	bandwidth limitations may	
	device, or until an interrupt	cause the adapter to	IBM Dictionary of
	generated by some other	underrun the network during	Computing (10th ed. 1993
	process occurs. If the	transmission, causing a	The return of part of the
	quantum is exhausted, the process is assigned a longer	partial frame with a guaranteed bad CRC to be	output of a machine, process, or system as inpu
	quantum and rejoins the	transmitted. If the value is	to the computer, especially
	queue. If the process	set too high, then	for self-correcting or conti
	initiates a transfer, its	unnecessary delays will be	purposes.
	quantum remains unaltered	incurred before the start of	purposes.
	and it rejoins the queue. If	transmission. The adapter	Microsoft Computer
	an externally generated	generates an indication of an	Dictionary (5th ed. 2002):
	interrupt occurs, the	underrun condition which is	The return of a portion of
	interrupt is serviced.	made available to the host	system output as input to t
	Servicing the interrupt may	through the XMIT	same system
	free some other process	FAILURE register. If such	Newton's' Telecom
	already in the queue, in	an underrun indication	Dictionary (fourth edition.
	which case that process may	occurs, then the host driver	<u>1991)</u>
	be preferentially restarted;	should increase the value on	Feedback: The return of pa

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and support
	evidence	evidence	evidence
	IBM Dictionary of	the XMIT START	of an output signal back to
	<u>Computing</u> (10th ed. 1993):	THRESH register. Further	the input side of the device
	The return of part of the	underrun indications should	Think of the high-pitched
	output of a machine,	cause the driver to	squeal you hear when
	process, or system as input	continually increase the	someone brings a
	to the computer, especially	XMIT START THRESH	microphone too close to t
	for self-correcting or control	value. If the XMIT START	loudspeaker. Not all
	purposes; Microsoft	THRESH value is increased	feedback is as obvious or
	Computer Dictionary (5th	to a value of greater than the	irritating. Some feedback
	ed. 2002): The return of a	maximum length expected	good.
	portion of system output as	by the system, then the early	
	input to the same system.	transmit start features	Newton's Telecom
	Often feedback is	should be disabled by	Dictionary (17th ed. 2001
	deliberately designed into a	writing a zero to the XMIT	The return of part of an
	system, but sometimes it is	START THRESH register."	output signal back to the
	unwanted. In electronics,	('872; Col. 29: 39-57).	input side of the device.
	feedback is used in	(3, 2, 23, 27, 37, 37, 37, 37, 37, 37, 37, 37, 37, 3	par since of the device.
	monitoring, controlling, and	"The XMIT FAILURE	EXPERT TESTIMONY:
	amplifying circuitry.	field contains the error code	
		that is made up of the status	Realtek's expert, Dr. Izha
	INTRINSIC EVIDENCE:	bits gathered from the	Rubin, may provide
	Claims: see, e.g., claim 19;	Ethernet transmitter after	testimony as to the
	("status information which	the completion of	definition of the disputed
	may be used by the host	transmission. This field is	terms as would be
	system as feedback for	mapped to the XMIT	understood by one of
	optimizing the threshold	FAILURE register for host	ordinary skill in the releva
	value"); see also claim 10;	access." ('872; Col. 14: 53-	art and may provide an
	Specification: see, e.g., figs.	57).	explanation of the
	2, 4, 13, 14, 17, 18; col.	37).	technology.
	2:31-34 ("the threshold	"XMIT FAILURE returns	technology.
	value may be set by the host	the cause of a transmit	
	system to optimize		
		failure. This register returns	
	performance using the alterable threshold store and	the cause of the failure of	
		the attempt(s) to transmit a	
	the posted status	queued frame. A non-zero	
	information"); see also Col.	value indicates that the	
	4: 56-60; Col. 29: 39-57;	frame encountered one or	
	Col. 14: 53-57; Col. 19: 14-	more errors during the	
	39; Col. 2: 27-34; see also	transmission attempt. The	
	Prosecution History: Office	bits in this register are	
	Action, Oct. 26, 1993, p. 5;	defined as follows: bit 0	
	Response to Office Action,	DMA UNDERRUN	
	Feb. 23, 1994, p. 2.	This register will contain	
		valid data regardless of the	
	EXTRINSIC EVIDENCE:	success or failure of the	
	3Com's expert, Dr. Michael	attempt to transmit a frame.	
	Mitzenmacher may provide	If there was no failure, then	
	an expert report or other	this register will contain a	
	form of testimony regarding	value of 0 (hex). The	
	the technology to which this	contents of this register are	
	term relates and how a	valid after the frame has	
	person having ordinary skill	completed transmission	
	in the art in the field of	(low byte of XMIT FRAME	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
	networking technology	STATUS not equal to ff	evidence
	would understand this term.	(hex)) and before XMIT	
	3Com reserves the right to	PROT ID is read. If a data	
	rely on testimony by any	underrun occurs, the adapter	
	expert in this action.	will force a CRC error into	
		the frame during	
	See also U.S. Patent Nos.	transmission to assure that	
	5,434,872; 5,732,094; 6,327,625; 6,526,446; and	the frame is received as a bad frame and is discarded	
	6,570,884; Joint Claim	by the destination device."	
	Construction Statement in	('872; Col. 19: 14-39).	
	Cv-05-00098 (VRW).		
		"In one aspect of the	
	3Com reserves the right to	invention, the monitoring	
	rely on any statement made by any party under the	logic includes a threshold store, which is	
	Patent Local Rules.	programmable by the host	
		computer for storing a	
		threshold value and logic for	
		posting status information to	
		the host. Thus, the	
		threshold value may be set by the host system to	
		optimize performance using	
		the alterable threshold store	
		and the posted status	
		information." ('872; Col. 2:	
		27-34).	
		PROSECUTION HISTORY:	
		PROSECUTION HISTORY.	
		Claim 10 of the '872	
		patent was amended to show	
		feedback for use by the host	
		system:	
		"	
		" control means, coupled with the network	
		interface means, for posting	
		status information [which	
		may be used] for use by the	
		host system, as feedback for	
		optimizing the threshold	
		value." ('872 prosecution history, Response mailed	
		February 23, 1994, p. 2).	
		EXTRINSIC EVIDENCE:	
		EXPERT TESTIMONY:	
		DI: 12	
		D-Link's expert, Howard	
		Frazier, may provide	<u> </u>

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		testimony as to the	
		definition of the disputed	
		terms as would be	
		understood by one of ordinary skill in the relevant	
		art and may provide an	
		explanation of the	
		technology.	
		DICTIONARY/TREATISE	
		DEFINITIONS:	
		N	
		Newton's Telecom	
		<u>Dictionary</u> , 19 <sup>th</sup> Ed., 2003,	
		pg. 319: Feedback - "The return of	
		part of an output signal back	
		to the input side of the	
		device."	
		Webster's Ninth New	
		Collegiate Dictionary,	
		(1986), pg. 454:	
		Feedback - "The return to	
		the input of a part of the	
		output of a machine, system, or process (as for producing	
		changes in an electronic	
		circuit that improve	
		performance or in an	
		automatic control device	
		that provide self-corrective	
		action)."	
"optimizing the	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
threshold"	Attempting to make the	Adjusting the current	Dynamically changing the
found in claim	transmission of frames more efficient.	threshold amount to make it as efficient, effective, or	threshold value by the host
numbers:	CITICICIII.	functional as possible.	system to make it as perfect effective, or functional as
maniovis.	DICTIONARY/TREATISE	Tuttetional as possible.	possible.
'872 patent: 10	DEFINITIONS:	EXTRINSIC EVIDENCE:	r
1	See "threshold value" in		INTRINSIC EVIDENCE:
also presented for	subsection 1 for definitions	DICTIONARY/TREATISE	
construction in:	of "threshold"; optimize:	DEFINITIONS:	'872 patent, Abstract; '094
(004	The American Heritage	*** 1	patent, Abstract ("The
'094 patent: 21	Dictionary of the English	Webster's Third New	monitoring logic includes a
	Language (4th ed. 2000):	International Dictionary	threshold store, which is
	Optimize: Computer	Unabridged (1981): "to	programmable by the host
	Science. To increase the	make as perfect, effective,	computer for storing a
	computing speed and	or functional as possible." p.1585	threshold value. Thus, the threshold value may be set
	efficiency of (a program), as by rewriting instructions;	p.1303	by the host system to
	see also Microsoft	WordNet 2.1 lexical	optimize performance in a
	Computer Dictionary (5th	database, Princeton Univ.	given setting.")
	Computer Dictionary (Juli	database, i iniccion oniv.	given sening.

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	ed. 2002): Optimization: 1.	(1991-2005) at	
	In programming, the process	http://wordnet.princeton.edu	'872 patent at 2:27-34; '09
	of producing more efficient	/perl/webwn; make optimal;	patent at 2: 21-27 ("In one
	(smaller or faster) programs	get the most out of; use best	aspect of the invention, the
	through selection and design	- 'optimize your resources';	monitoring logic includes
	of data structures. 2. The	modify to achieve	threshold store, which is
	process of a compiler or	maximum efficiency in	programmable by the host
	assembler in producing	storage capacity or time or	computer for storing a
	efficient executable code.	cost - 'optimize a computer	threshold value and logic
		program'"	for posting status
	INTRINSIC EVIDENCE:		information to the host.
	Claims: claim 10; claim 19;	D-Link also incorporates by	Thus, the threshold value
	Specification: figs. 2, 4, 13,	reference Realtek's	may be set by the host
	14, 17, 18; col. 29:35-38	references.	system to optimize
	("If this register set to zero,		performance using the
	then the early transmit		alterable threshold store
	feature is disabled and the		and the posted status
	entire transmit frame must		information.")
	reside on the adapter before		
	the adapter will begin to		'872 patent at 4:46-55; '09
	transmit it"); col. 29:48-51		patent at 4:38-46 ("The
	("If such an underrun		threshold store 43, in a
	indication occurs, then the		preferred system, is
	host driver should increase		dynamically programmable
	the value on the XMIT		by the host computer 30. In
	START THRESH		this embodiment, the
	register"); see also col.		threshold store 43 is a
	29:12-57; col. 4:46-55; col.		register accessible by the
	2:27-34; col. 2:31-34; col.		host through the interface
	4:58-60; col. 29:39-40; <u>see</u>		logic 31. Alternatively, the
	also Prosecution History:		threshold store may be a
	Office Action, Oct. 26,		read only memory set duri
	1993, p. 4; Office Action,		manufacture. In yet other
	Oct. 26, 1993, p. 5; Part 131		alternatives, the threshold
	Affidavit, p. Ex. 1, p. 6;		store may be implemented
	Response to Office Action,		using user specified data in
	Feb. 23, 1994, p. 2.		non-volatile memory, such
			as EEPROMs, FLASH
	EXTRINSIC EVIDENCE:		EPROMs, or other memory
	3Com's expert, Dr. Michael		storage devices.")
	Mitzenmacher may provide		
	an expert report or other		'872 patent at 29:12-57;
	form of testimony regarding		'094 patent at 27:44-28:-1
	the technology to which this		("XMIT START THRESH
	term relates and how a		is used to specify the
	person having ordinary skill		number of bytes of the
	in the art in the field of		transmit frame that must
	networking technology		reside on the adapter,,
	would understand this term.		before the adapter can
	3Com reserves the right to		commence with the media
	rely on testimony by any		access control functions
	expert in this action.		associated with transmitting
			the frame.

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
	See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).  3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		The value for this register may be programmed by the host to optimize performance The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register. Further underrun indications
			should cause the driver to continually increase the XMIT START THRESH value ")
			DICTIONARY/TREATISE DEFINITIONS: See "altering the
			threshold" for definitions of "threshold."
			Optimize:
			Webster's Ninth New Collegiate Dictionary, (ninth edition, 1988) Optimize: to make as perfect, effective, or
			functional as possible.  EXPERT TESTIMONY:
			Realtek's expert, Dr. Izhak
			Rubin, may provide testimony as to the definition of the disputed
			terms as would be understood by one of
			ordinary skill in the relevant art and may provide an explanation of the technology.
"threshold value" found in claim	PROPOSED CONSTRUCTION: A value representing the quantity of data sufficient to	PROPOSED CONSTRUCTION: A set value indicating a desired limit.	PROPOSED CONSTRUCTION: A number corresponding to a level of data required for
numbers:	trigger the initiation of	domed milit.	some process to take place.

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construction and supporting evidence widence construction and supporting evidence widence evidence evi					
evidence evidencion evidence evidence evidence evidence evidence evidence evidence evidence evidence evidence evidence evidence evidence evidencion evidence evidencions evidence evidencions evidence evidence evidencions evidence evidencions evidence evidencions evidence evidencions evidence evidencions evidence evidencions evidence evidencions evidence evidencions evidence evidencions evidence ev	1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
Transmission  Transmission  See 'threshold value' in subsection 1 for definitions of "threshold."  The following citations support D-Link's proposed claim construction.  "Coupled with the threshold logic 36 is a threshold logic 36 is a threshold logic 36 is a threshold store 43 which stores a threshold value which indicates an amount of data of a frame that must be resident in the frame when the threshold determination indicates that a sufficient portion of the frame when the threshold determination indicates that a sufficient portion of the frame into the transmit buffer," and prior to the transmit buffer," and prior to the transmit buffer, and prior to the transmit buffer, and prior to the transmit buffer, and prior to the transmit buffer," see also col. 2: 27-34; col. 4:40-45; col. 2: 27-34; col. 4:40-45; col. 2: 2-29. (2. 2) (2. 2) (2. 2) (2. 2) (2. 2) (2. 2) (2. 2) (2. 2) (2. 3) (2. 2) (2. 3) (2. 2) (2. 3) (2. 2) (2. 3) (2. 2) (2. 3) (2. 2) (2. 3) (	ار	(disputed terms in <b>bold</b> )			11 0
3   S72 patent: 10	2				evidence
also presented for construction in:  5   See "Threshold value" in subsection 1 for definitions of "threshold."  7   1094 patent: 47   Netter 1   1094 patent: 47   Netter 1   1094 patent: 48   Netter 1   1094 patent: 49   Netter 1   Netter	2	'872 natent: 10	transmission	KEFERENCES.	DICTIONARY/TREATISE
also presented for construction in:  3 between the form of the first subsection 1 for definitions of "threshold!"  7 colly a patent: 4 delay p	د	672 patent. 10	DICTIONARY/TREATISE	PATENT SPECIFICATION:	
subsection I for definitions of "threshold."  7	4	also presented for	· · · · · · · · · · · · · · · · · · ·		
- 459 patent: 1  - 994 patent: 47  - 994 patent: 47  - 994 patent: 47  - 1994 patent: 47	.				
"Coupled with the threshold logic 26 is a threshold store 43 which stores a threshold value which indicates an amount of data of a frame that me may be imitiated by the transmit Duffer, and prior to the transfer of all of the data of the frame is resident in the transmit buffer, in general col. 12:27-34; col. 4:40-45; col. 19:3-5; col. 26:69-9; col. 29:28-31; Col. 2: 49-55; Col. 21: 23-9; Col. 3: 69-65; Col. 4: 40-45; see also Prosecution History. Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Act	5			claim construction.	
Section   Claim   Section   Claim   Section   Claim   Section   Claim   Section   Section   Claim   Section   Sect		'459 patent: 1	of "threshold."		
Claims: claim 5; claim 6; claim 6; claim 19; claim 19; claim 6 23; claim 24; Specification: see, e.g., figs. 11-17; col. 2:22-27 ("The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit DMA logic and MAC 39." ("872; Col. 4: 40-45) (emphasis added).  The American Heritage Dictionary of the English Language (4th ed. 2000) The point that must be resident in the frame in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer."); see also col. 2:7-34; col. 4: 40-43; col. 4: 40-43; col. 4: 40-43; col. 4: 40-43; col. 4: 40-45; see also col. 2:7-34; col. 4: 40-45; see also Col. 2: 12-39; col. 2: 66-9; col. 4: 40-45; see also Posecution History. Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Cet. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2.  EXTRINSIC EVIDENCE: 3Com 8 expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3 Com reserves the right to rely on testimony by any expert in this action.	6	6004 4 47	T		` /
claim 10; claim 19; claim 23; claim 24; Specification; see, e.g., figs. 11-17; col. 2:22-27 ("The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame into the transmit buffer,") see also col. 2:27-34; col. 4:40-45; col. 19:3-5; col. 2:6:6-9; col. 29:28-31; Col. 2: 49-55; Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also Prosecution History. Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology would understand this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 260 reserves the right to rely on testimony by any expert in this action.  stores a threshold value which indicates an amount of data of a frame that must be resident in the frame that must be resident in the frame that must be resident in the frame that must be resident in the frame that must be resident in the frame way be initiated by the transmission of that frame may be initiated by the transmit logic and MAC 39." (872; Col. 4: 40-45) the frame into the transmit logic and the buffer 34, then the threshold as the resident in the buffer 34, then the threshold as from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing a to the computer 30 into the buffer 34 is larger than the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired." (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  The American Heritage Dictionary of the English Language (4th ed. 2000)  The English Language (4th ed. 2000)  The English Language (4th ed. 2000)  The English Language (4th ed. 2000)  The English Language (4th ed. 2000)  The English Language (4th ed. 2000)  The Engl		1094 patent: 47			
23; claim 24; Specification: see_e.g., fiss. 11-17; col. 2:22-27 ("The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmission of the frame is resident in the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of that frame may be initiated by the transmission of the frame when the transmist buffer 34, better 18, 20, 20, 21, 21, 20, 20, 31, 51, 59, 65; col. 4: 68-Col. 5: 13, 60, 19, 21, 20, 20, 21; 20, 20, 21; 20, 20, 20, 21; 20, 20, 20, 20, 20, 20, 20, 20, 20, 20,	7				
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a sufficient portion of the frame is resident in the transmit buffer, and prior to the transmit buffer, and prior to the transmit buffer, and prior to the transmit buffer."); see also col. 2:27-34; col. 4:40-45; col. 9:3-5; col. 26:6-9; col. 29:28-31; Col. 2: 49-55; Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2.  21  22  23  24  25  26  26  27  27  28  29  20  20  21  21  22  23  24  25  26  26  27  27  27  28  29  20  20  20  21  21  22  23  23  24  25  26  26  27  27  28  29  20  20  20  21  21  22  23  24  25  26  26  27  27  27  28  29  20  20  20  20  21  21  22  23  24  25  26  26  27  28  29  20  20  20  20  20  20  20  20  20	11				
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the transfer of all of the data of the frame into the transmit buffer; '); see also col. 2:27-34; col. 4:40-45; col. 19:3-5; col. 26:6-9; col. 29:28-31; Col. 2: 49-55; Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also col. 20: 12: 12-39; Col. 3: 59-65; Col. 2: 66; Col. 2: 12: 239; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also col. 20: 10: 20: 20: 20: 20: 20: 20: 20: 20: 20: 2				"When the <i>threshold</i>	
transmit buffer."); see also col. 2:27-34; col. 4:40-45; col. 19:3-5; col. 26:6-9; col. 29:28-31; Col. 2: 49-55; Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2.  19  20  21  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transmit logic 39 is available to transmit the transmit logic 39 is available to transmit logic 39 is also called a limen. 2. The least value of a current, voltage, or other quantity that produces the minimum detectable response. It is also called a limen. 2. The entire frame has been transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the thresho	13			amount of data is resident in	McGraw-Hill Electronics
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col. 19:3-5; col. 26:6-9; col. 29:28-31; Col. 2: 49-55; Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Feb. 23, 1994, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3 Com reserves the right to rely on testimony by any expert in this action.  col. 19:2-9; Col. 2: 49-55; Col. 2: 49-55; Col. 2: 6-9; col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 68-Col. 5: 13; cor other quantity that produces the minimum detectable response. It is also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation.  The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34 is larger than the buffer 34 is larger than the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  EXPERT TESTIMONY:  (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  EXPERT TESTIMONY:  (*872; Col. 4: 68-Col. 5: 13) (emphasis added).	14				
29:28-31; Col. 2: 49-55; Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Feb. 23, 1994, p. 2.  20  21  22  23  24  25  26  27  28  29  29  20  20  20  20  20  21  22  22  23  24  25  26  26  27  28  29  29  20  20  20  20  20  20  20  20	1				
Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also OProsecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  Col. 4: 40-45; see also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation.  Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Oct. 26, 1994, p. 2.  EXTRINSIC EVIDENCE: 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  EXPERT TESTIMONY:	13				
65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Cot. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  The burler 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired." (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the defentition of the disputed	16				
transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame being downloaded into the buffer 30 computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold set by the threshold set by the threshold set by the threshold set by the threshold set by the threshold set by the threshold set by the threshold set by the threshold set by the threshold set of the data is desired."  24 person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  25 procedure 42, This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing downloaded into the buffer 34 is larger than the threshold set by the threshold set by the threshold set by the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing downloaded into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame bate provide an expert report or other frame has been transferred from the host computer 30, the frame bate provide and social also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation.					
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Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  26 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  27 3Com reserves the right to rely on testimony by any expert in this action.  Office Action, Oct. 26, 1993, p. 5; Response to Coffice Action, Feb. 23, 1994, p. 2.  EXTRINSIC EVIDENCE: 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold set by the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed			· ·		
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20 1994, p. 2.  21 2					oscillation.
20 1994, p. 2.  21 2	19				
is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  22 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  23 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  24 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  25 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  26 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  27 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  28 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  29 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  20 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  21 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  22 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  23 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  24 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  25 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  26 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  27 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  28 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  29 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  20 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  20 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  21 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  29 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  20 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  21 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  22 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  23 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  24 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  25 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  26 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  27 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  28 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).**  29 (**872; Col. 4: 68-Col. 5: 13) (emphasis added).*					threshold value
EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired." ('872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed	20		1994, p. 2.		<u></u>
3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  3Com reserves the right to rely on testimony by any expert in this action.  3Com's expert, Dr. Michael Mitzenmacher may provide an expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  3Com reserves the right to rely on testimony by any expert in this action.  3Com reserves the right to rely on testimony by any expert in this action.  4download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  EXPERT TESTIMONY:  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed	ر 1 ا		EXTRINSIC EVIDENCE:		McGraw-Hill Electronics
22 an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  25 a Com reserves the right to rely on testimony by any expert in this action.  26 an expert report or other buffer 34 is larger than the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  ('872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed	41				
form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  3Com reserves the right to rely on testimony by any expert in this action.  an expert report of other form of testimony regarding the technology to which this term shold set by the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  ('872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed	$_{22}\ $			*	
the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  3Com reserves the right to rely on testimony by any expert in this action.  threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  ('872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed					
term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.  3Com reserves the right to rely on testimony by any expert in this action.  threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired."  ('872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed	23				
person having ordinary skill in the art in the field of networking technology would understand this term.  3Com reserves the right to rely on testimony by any expert in this action.  State of the data is desired."  ('872; Col. 4: 68-Col. 5: 13)  (emphasis added).  Weather the computer 30 indicates that immediate transmission of the data is desired."  ('872; Col. 4: 68-Col. 5: 13)  (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed					-
in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  that immediate transmission of the data is desired." ('872; Col. 4: 68-Col. 5: 13) (emphasis added).  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed	24			I	
networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  of the data is desired." ('872; Col. 4: 68-Col. 5: 13) (emphasis added).  rely on testimony by any expert in this action.  "FIG. 1 illustrates a data communication system  EXPERT TESTIMONY:  Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed	_		1 0 1		
would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  (*872; Col. 4: 68-Col. 5: 13) (emphasis added).  (*FIG. 1 illustrates a data communication system  (*FIG. 1 illustrates a data definition of the disputed)	25				EXPERT TESTIMONY:
rely on testimony by any expert in this action.  Rubin, may provide testimony as to the communication system  Rubin, may provide testimony as to the definition of the disputed	<u>,</u>				D 1/12
expert in this action.  "FIG. 1 illustrates a data communication system testimony as to the definition of the disputed	26			(emphasis added).	
communication system definition of the disputed	$_{27}$			"FIG 1 illustrates a data	
	4 / <b> </b>		expert in this action.		
	28		<u> </u>	communication system	

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
(	evidence	evidence	evidence
	See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and	according to the present invention with a controller circuit using a dedicated	terms as would be understood by one of ordinary skill in the relevan
	6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).	transmit buffer memory which is automatically enabled to begin transmission of a frame on	art and may provide an explanation of the technology.
	3Com reserves the right to rely on any statement made	the network when the number of bytes available in	
	by any party under the Patent Local Rules.	the transmit buffer memory exceeds a preprogrammed <i>threshold.</i> " ('872; Col. 3:	
		59-65) (emphasis added).	
		"XMIT START THRESH provides for an early start of transmission. The XMIT	
		START THRESH register is used to specify the number of transmit bytes that must	
		reside on the adapter before it will start transmission.	
		Values greater than the maximum frame length will prevent this function from	
		operating properly. The method for disabling this function is to set the register	
		to zero. Bytes are counted starting with the first byte of the destination field of the	
		transmit frame. The number of bytes considered to be	
		available is the sum of the immediate data written to XMIT AREA by the host	
		and those bytes transferred to the transmit data buffers in the adapter using bus	
		master DMA operations. The transmit request will be	
		posted immediately after XMIT START THRESH transmit frame bytes are	
		made available from the immediate data or when the adapter has bus-mastered	
		XMIT START THRESH- XMIT IMMED LEN bytes	
		onto the adapter. The number of bytes resident on the adapter must be equal to	
		or greater than the value in	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence XMIT START THRESH	evidence
		for the transmission to	
		commence, unless the total	
		frame size is less than	
		XMIT START THRESH.	
		In that case, the frame will	
		begin transmission when the	
		entire frame has been copied	
		to the adapter. The actual	
		transmission of the frame	
		may be delayed by previous	
		pending transmit frames and	
		by deferrals to network	
		traffic. This register is set to zero during a reset."	
		('872; Col. 21: 12-39)	
		(0/2, Coi. 21. 12-39)	
		"The threshold logic	
		determines the amount of	
		immediate data from the	
		descriptor, and monitors the	
		downloading of data of the	
		frame into the download	
		area. When the	
		combination meets the	
		threshold, then actual	
		transmission of the frame is	
		initiated. Thus, transmission of a frame may	
		be initiated before the	
		complete frame has been	
		downloaded into the	
		download area." ('872; Col.	
		2: 49-55) (emphasis added).	
		, , ,	
		DICTIONARY/TREATISE	
		DEFINITIONS:	
		Webster's Ninth New	
		Collegiate Dictionary	
		(1983), pg.229:	
		Threshold - "A level, point,	
		or value above which	
		something is true or will	
		take place and below which	
		it is not or will not."	
		EXPERT TESTIMONY:	
		D. T. I.	
		D-Link's expert, Howard	
		Frazier, may provide	
		testimony as to the definition of the disputed	
	1	r accumion or me dispilled	İ

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
		terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the	
		technology.	
"logic which initiates transmission of the	PROPOSED CONSTRUCTION: Threshold logic that begins	Refer to the construction under 35 U.S.C. § 112 ¶ 6 in	Please refer to the construction under 35 U.S.C
frame when no complete frame of	transmission of a frame before all the data in the	Section B.	§ 112 ¶ 6. To the extent this term requires construction,
data is present in the buffer memory"	frame is within the buffer memory.		Realtek asserts that "logic" should be construed as
found in claim numbers:	DICTIONARY/TREATISE DEFINITIONS: See "logic,"		"means" and, therefore, this claim element should be governed by 35 U.S.C. § 112
'872 patent: 21	"frame" and "buffer" in subsection 1 for definitions of those terms, respectively,		¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, the claim
	"data value" in subsection 6 for definitions of "data,"		limitation should be construed as "device that
	and " <b>buffer memory</b> " in subsection 1 for definitions of "memory;" <u>transmission</u> :		initiates transmission of the frame when no complete frame of data is present in
	The American Heritage Dictionary of the English		the buffer memory."
	Language (4th ed. 2000): The act or process of		
	transmitting. The fact of being transmitted. transmit: To pass along (news or		
	information); communicate. initiate: The American		
	Heritage Dictionary of the English Language (4th ed.		
	2000): To set going by taking the first step; begin: initiated trade with		
	developing nations. See Synonyms at begin. To		
	introduce to a new field, interest, skill, or activity.		
	To admit into membership, as with ceremonies or ritual. Initiated or admitted, as to		
	membership or a position of authority. Instructed in		
	esoteric knowledge. Introduced to something		
	new. One who is being or has been initiated. One who has been introduced to or has attained knowledge in a		

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
3		particular field.		
		INTRINSIC EVIDENCE:		
4		Claims: claim 1; claim 21;		
_		Specification: see, e.g., figs.		
5		1, 2, 4, 4A, 5, 9, 11-18; col. 2:22-27 ("The network		
6		interface controller includes		
		logic for initiating		
7		transmission of the frame when the threshold		
8		determination indicates that		
8		a sufficient portion of the		
9		frame is resident in the transmit buffer, and prior to		
10		the transfer of all of the data		
10		of the frame into the		
11		transmit buffer."); see also col. 4:40-45; see also		
		Prosecution History: Part		
12		131 Affidavit, pp. 2-3;		
13		Response to Office Action, Oct. 5, 1994, p. 2; Response		
13		to Office Action, Oct. 5,		
14		1994, p. 3.		
15		EXTRINSIC EVIDENCE:		
13		3Com's expert, Dr. Michael		
16		Mitzenmacher may provide		
		an expert report or other form of testimony regarding		
17		the technology to which this		
18		term relates and how a		
		person having ordinary skill in the art in the field of		
19		networking technology		
20		would understand this term.		
20		3Com reserves the right to rely on testimony by any		
21		expert in this action.		
22				
22		See also U.S. Patent Nos. 5,434,872; 5,732,094;		
23		6,327,625; 6,526,446; and		
		6,570,884; Joint Claim		
24		Construction Statement in		
25		Cv-05-00098 (VRW).		
		3Com reserves the right to		
26		rely on any statement made		
27		by any party under the Patent Local Rules.		
41		Tatont Loom Ituios.	<u> </u>	

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#### 3. <u>U.S. Pat. No. 5,732,094</u>

4				
_	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
3	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
		evidence	evidence	evidence
4	"buffer"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	Same as "buffer memory"
		A memory for temporary	Term is used only in phrase	identified above.
5	found in claim	storage of data.	"buffer memory." See	
	numbers:		construction of "buffer	
6		DICTIONARY/TREATISE	memory."	
	'094 patent: 1, 9, 21,	<u>DEFINITIONS</u> : <u>See</u> " <b>buffer</b> "		
7	28, 39, 47	in subsection 1.		
8	also presented for	INTRINSIC EVIDENCE:		
	construction in:	Claims: see, e.g., claim 33		
9		("The method as in claim		
1	'459 patent: 1	28, wherein the initiating		
10		transmission of the frame		
-	'872 patent: 1, 10, 21	step includes: retrieving		
11		data from the buffer		
^ ^		memory; and supplying the		
12		retrieved data for		
12		transmission to the network		
13		transceiver."); see also		
13		claim 1; claim 4; claim 6;		
14		claim 7; claim 9; claim 10;		
14		claim 11; claim 14; claim		
15		16; claim 20; claim 21;		
13		claim 28; claim 29; claim		
16		30; claim 34; claim 38;		
10		claim 39; claim 41; claim		
17		44; claim 45; claim 47;		
17		claim 49; claim 52;		
1.0		Specification: see, e.g., figs.		
18		2, 6-10E; col. 1:44-50 ("Transmit data buffers are		
1.		to be distinguished from		
19		first-in-first-out FIFO		
		systems in which the		
20		sending system downloads		
$\  \cdot \ $		data of a frame into the		
21		FIFO, while the network		
_		adapter unloads the FIFO		
22		during a transmission.");		
		col. 2:28-30 ("the transmit		
23		data buffer includes a		
		transmit descriptor ring, and		
24		a transmit data buffer") and		
		other quotes from "buffer"		
25		in subsection 2 above,		
		which also appear in the		
26		specification of the '094,		
		since it is a continuation of		
27		the '872; see also col. 1:29-		
- 1		, , , , , , , , , , , , , , , , , , , ,	ı	1

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	33; col. 1:35-37; col. 1:38-		
	50; col. 1:51-56; col. 1:56-		
	58; col. 1:60-62; col. 2:3-5;		
	col. 2:7-9; col. 2:11-20; col.		
	2:35-39; col. 3:14-33; col. 4:55-5:12; col. 5:31-32; col.		
	5:45-47; col. 6:20-22; col.		
	8:31-33; col. 8:34-37; col.		
	8:44-46; col. 8:48-51; col.		
	8:53-56; col. 8:58-61; col.		
	8:66-9:3; col. 9:8-10; col.		
	9:33-35; col. 9:38-43; col.		
	9:50-54; col. 9:56-59; col.		
	10:50-53; col. 10:55-58; col.		
	10:65-67; col. 11:1-4; col.		
	11:23-25; col. 11:34-37;		
	col., 12:4-8; col. 12:18-28;		
	col. 12:30-36; col. 12:39-41;		
	col. 12:44-52; col. 12:54-		
	13:5; col. 13:9-11; col.		
	13:17-21; col. 13:39-47; col.		
	14:52-54; col. 14:57-59; col.		
	15:8-10; col. 15:16-18; col.		
	15:20-22; col. 15:24-27; col.		
	15:42-45; col. 15:48-52; col.		
	15:64-67; col. 16:11-14; col.		
	16:18-22; col. 16:23-33; col.		
	16:35-42; col. 16:44-48; col.		
	16:63-65; col. 17:6-9; col.		
	17:30-34; col. 17:51-52; col.		
	17:55-58; col. 18:47-50; col. 20:19-22; col. 20:39-41; col.		
	20:56-57; col. 20:63-66; col.		
	20:67-21:3; col. 21:15-18;		
	col. 21:22-27; col. 21:39-45;		
	col. 21:47-50; col. 21:59-64;		
	col. 22:33-35; col. 22:38-41;		
	col. 22:49-53; col. 23:13-18;		
	col. 23:24-27; col. 23:25-28;		
	col. 23:28-31; col. 23:33-37;		
	col. 24:27-30; col. 27:16-19;		
	col. 27:39-42; col. 27:57-61;		
	see also Prosecution		
	History: Specification as		
	Filed, p. 52; Specification as		
	Filed, p. 53; Specification as		
	Filed, p. 54; Specification as		
	Filed, p. 55; Specification as		
	Filed, p. 56; Specification as		
	Filed, p. 57; Preliminary		
	Amendment, Mar. 3, 1995,		
	p. 2; Preliminary		
	Amendment, Mar. 3, 1995,		

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_ ₁	Claire Income	201	D. Lindy many 1	D14-1-2 1
1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
4		p. 6; Office Action, Mar. 19,	evidence	evidence
3		1996, p. 2; Office Action,		
د		Mar. 19, 1996, p. 3; Office		
4		Action, Mar. 19, 1996, p. 4;		
7		Office Action, Mar. 19,		
5		1996, p. 5; Office Action,		
		Mar. 19, 1996, p. 6; Office		
6		Action, Mar. 19, 1996, p. 7;		
		Office Action, Mar. 19,		
7		1996, p. 8; Office Action,		
1		Jan. 7, 1997, p. 2; Response		
8		to Office Action, Apr. 7,		
		1997, pp. 1-2; Response to Office Action, Apr. 7, 1997,		
9		p. 5.		
		P. J.		
10		EXTRINSIC EVIDENCE: See		
_,		section I.A, supra (agreed		
11		upon definition for "buffer"		
12		in '625 and '884 patents);		
12		3Com's expert, Dr. Michael		
13		Mitzenmacher may provide		
13		an expert report or other form of testimony regarding		
14		the technology to which this		
17		term relates and how a		
15		person having ordinary skill		
		in the art in the field of		
16		networking technology		
		would understand this term.		
17		3Com reserves the right to		
		rely on testimony by any		
18		expert in this action.		
		See also U.S. Patent Nos.		
19		5,434,872; 5,732,094;		
		6,327,625; 6,526,446; and		
20		6,570,884; Joint Claim		
21		Construction Statement in		
21		Cv-05-00098 (VRW).		
22				
		3Com reserves the right to		
23		rely on any statement made		
دے		by any party under the Patent Local Rules.		
24	"buffer memory"	Proposed Construction:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
- '	bullet memory	A memory for temporary	Dedicated random access	A memory that (1) stores
25	found in claim	storage of data.	memory that (1) stores	frame data such that the
-	numbers:		transmit data, (2) is distinct	frame data can be retrieved
26		DICTIONARY/TREATISE	from a FIFO, (3) can always	independently of the order
	'094 patent: 1, 9, 21,	DEFINITIONS:	retransmit a frame of data	in which the frame data
27	28, 39, 47	See "buffer memory" in	without having to retrieve it	were stored and the frame
- 11				

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
٦	-1	subsection 1.	from a host, and (4) is	data can always be retained
3	also presented for construction in:	INTERNICIO EVIDENCE:	controlled independently of	and reused and can be accessed by the host system;
4	construction in:	INTRINSIC EVIDENCE: Claims: see, e.g., claim 33	the host system.	and (2) is not a first-in-first-
4	'459 patent: 1	("The method as in claim	REFERENCES:	out (FIFO) system.
5	+37 patent. 1	28, wherein the initiating	KEFERENCES.	out (1 ii 0) system.
3	'872 patent: 1, 10, 21	transmission of the frame	PATENT SPECIFICATION:	INTRINSIC EVIDENCE:
6	0,2 pavenu 1, 10, 21	step includes: retrieving	THE STEEL ST	in that the bottom is a second
6		data from the buffer	Claim 2 of the '872 patent,	'872 patent at 1:47-54; '094
7		memory; and supplying the	the parent of the '094	patent at 1:44-50 ("Transmit
′		retrieved data for	patent, recites "The	data buffers are to be
8		transmission to the network	apparatus of claim 1,	distinguished from first-in-
8		transceiver."); see also	wherein the <i>transmit buffer</i>	first-out FIFO systems, in
9		claim 1; claim 2; claim 4;	includes" (emphasis	which the sending system
		claim 6; claim 7; claim 9;	added).	downloads data of a frame
10		claim 10; claim 11; claim		into the FIFO, while the
		14; claim 16; claim 20;	Claim 7 of the '872 patent,	network adapter unloads the
11		claim 21; claim 28; claim 29; claim 30; claim 33;	the parent of the '094	FIFO during a transmission.  The data in FIFOs cannot
		claim 34; claim 38; claim	patent, recites "The	be retained and reused by
12		39; claim 41; claim 44;	apparatus of claim 1,	the media access control
		claim 47; claim 49; claim	wherein the <i>buffer</i> includes	functions, or by the host,
13		52; Specification: see, e.g.,	a transmit descriptor ring	like data in transmit data
		col. 1:44-50 ("Transmit data	buffer and a transmit data	buffers.")
14		buffers are to be	buffer" (emphasis	
		distinguished from first-in-	added).	'872 patent at 1:65-2:2; '094
15		first-out FIFO systems in	"Forly initiation of	patent at 1:60-65
		which the sending system	"Early initiation of transmission of data in a	("Furthermore, the prior art
16		downloads data of a frame	network interface that	systems which use transmit
		into the FIFO, while the network adapter unloads the	includes a dedicated	data buffers require the host or sending system to
17		FIFO during a	transmit buffer is provided	manage the transmit data
1.0		transmission."); col. 2:28-30	in a system which includes	buffer. A network interface
18		("the transmit data buffer	logic for transferring frames	controller transfers data
10		includes a transmit	of data composed by the	from the host managed
19		descriptor ring, and a	host computer into the	transmit data buffer using
20		transmit data buffer") and	transmit buffer." ('872	DMA techniques through a
20		other quotes from "buffer"	Abstract and '094 Abstract) <sup>3</sup>	FIFO buffer in the interface
21		in subsection 2 above,	(emphasis added).	controller and on to the
_		which also appear in the	"The present invention	network.")
22		specification of the '094, since it is a continuation of	provides for the early	'872 patent at 2:7-10; '094
		the '872; see also col. 2:3-5;	initiation of transmission of	patent at 2:3-5 ("It is
23		col. 2:28-52; col. 1:60-65;	data in a network interface	desirable to provide the
_		col. 1: 34-50; col. 1: 51-58;	that includes a <i>dedicated</i>	advantages of a transmit
24		col. 1: 60-65; col. 1: 66 -	transmit buffer. The system	data buffer, while
		col. 2:2; col. 12: 45-53; col.	includes logic for	maintaining the
25		12: 54-63; col. 12: 64 -	transferring frames of data	communications throughput
		col.13: 5; col. 2: 8-12; col.	composed by the host	available from the simpler
26				
- 11	13			

<sup>&</sup>lt;sup>3</sup> Citations to the description of the '872 patent can also be found in the description of the related '094 patent; all citations to the '872 patent apply equally to the '094 patent.

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	3:50-52; col. 5:45-47; <u>see</u>	computer into the transmit	FIFO based systems.")
	also Prosecution History:	buffer." ('094; Col. 2: 8-12)	1050
	Specification as Filed, p. 52;	(emphasis added).	'872 patent at 2:35-55; '09
	Specification as Filed, p. 54;		patent at 2:28-52
	Specification as Filed, p. 55;	"According to another	("According to another
	Specification as Filed, p. 56;	aspect of the present	aspect of the present
	Specification as Filed, p. 57;	invention, the <i>transmit</i>	invention, the transmit
	Preliminary Amendment,	buffer includes a transmit	buffer includes a transmit
	Mar. 3, 1995, p. 2;	descriptor ring, and a	descriptor ring, and a
	Preliminary Amendment,	transmit data buffer. The	transmit data buffer
	Mar. 3, 1995, p. 6; Office	host system composes a	
	Action, Mar. 19, 1996, p. 2;	frame by storing a transmit	'872 patent at 13:17-48;
	Office Action, Mar. 19,	descriptor in the adapter	'094 patent at 12:44-13:5
	1996, p. 3; Office Action,	managed transmit descriptor	("A. Transmit Data Buffer
	Mar. 19, 1996, p. 4; Office	ring." ('094; Col. 2: 28-32)	
	Action, Mar. 19, 1996, p. 6;	(emphasis added).	The transmit data buffer
	Office Action, Mar. 19,		occupies 3K bytes as
	1996, p. 7; Office Action,	"Some network adapter	mentioned above. This
	Jan. 7, 1997, p. 2; Response	interfaces include dedicated	region is divided into two
	to Office Action, Apr. 7,	transmit buffers into which	1.5K buffers. Only the dat
	1997, pp. 1-2; Response to	a frame of data composed	that are downloaded to the
	Office Action, Apr. 7, 1997,	by the sending system can	adapter via bus master
	p. 5.	be downloaded by the	transfers are stored in thes
		sending system. The frame	buffers. The controller wi
	EXTRINSIC EVIDENCE: See	is then stored in the <i>transmit</i>	use both the contents of th
	section I.A, supra (agreed	data buffer until the media	transmit data buffer and th
	upon definition for "buffer"	access control functions	immediate data portion of
	in '625 and '884 patents).	associated with transmitting	the transmit descriptors,
	3Com's expert, Dr. Michael	the frame on the network	when encapsulating a fran
	Mitzenmacher may provide	have successfully	for transmission
	an expert report or other	transmitted the frame, or	The transmit buffers are
	form of testimony regarding	cancelled the frame	shared by the download
	the technology to which this	transmission. If the frame	DMA logic and the transn
	term relates and how a	transmission is cancelled,	DMA logic. The transmit
	person having ordinary skill	the data may be retained in	DMA logic may switch
	in the art in the field of	the transmit data buffer	from buffer 0 to buffer 1
	networking technology	until the sending system	and back again freely. The
	would understand this term.	initiates a second attempt to	only restriction being the
	3Com reserves the right to	transmit the frame.	availability of transmit da
	rely on testimony by any	Transmit data buffers are to	as defined by the transmit
	expert in this action.	be distinguished from first-	start threshold register
	San also II C. Datant Nac.	in-first-out FIFO systems, in	.")
	See also U.S. Patent Nos.	which the sending system	(972 notant at 1.5 14
	5,434,872; 5,732,094;	downloads data of a frame	'872 patent, at 1:5-14
	6,327,625; 6,526,446; and	into the FIFO, while the	("CROSS-REFERENCE
	6,570,884; Joint Claim	network adapter unloads the	TO RELATED
	Construction Statement in	FIFO during a transmission.	APPLICATIONS
	Cv-05-00098 (VRW).	The data in FIFOs cannot be	The present application is
		retained and reused by the	related to copending U.S.
	3Com reserves the right to	media access control	patent application entitled
	rely on any statement made	functions, or by the host,	NETWORK INTERFACE
	by any party under the	like data in transmit data	WITH HOST
	Patent Local Rules.	buffers." ('094; Col. 1: 34-	INDEPENDENT BUFFEI

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
⁴∭		evidence	50) (emphasis added).	MANAGEMENT,
3			(***	application Ser. No.
			"Although transmit data	07/921,519, filed 28 Jul.
4∭			buffers enable a sending	1992, now U.S. Pat. No.
_			system to compose and download a frame into the	5,299,313, which was owned at the time of
5			transmit data buffer, and	invention and is currently
6			then attend to other tasks	owned by the same
<b>_</b>			while the network adapter	assignee.")
7			attempts to transmit the	(450 1.5.12
			frame, it suffers the disadvantage that	'459 patent, at 1:5-13 ("CROSS-REFERENCE
3			transmission of a frame is	TO RELATED
$\  \ $			delayed until the entire	APPLICATIONS
9			frame has been downloaded	The present application is
)			into the buffer. Thus,	related to copending U.S.
<b>^</b>			transmit data buffer type	patent application entitled NETWORK INTERFACE
1			systems improve host system efficiency at the	WITH HOST
			expense of network	INDEPENDENT BUFFER
2			throughput." ('094; Col. 1:	MANAGEMENT, Ser. No.
$\ $			51-58) (emphasis added).	07/921,519, filed Jul. 28,
3			45 41	1992, which was owned at the time of invention and is
$_{4}$			"Furthermore, the prior art systems which use <i>transmit</i>	currently owned by the
۱			data buffers require the host	same assignee.")
5			or sending system to	
			manage the transmit data	'459 patent, at 13:58-14:22
5			buffer. A network interface	("A. Transmit Data Buffer
-∭			controller transfers data from the host managed	The transmit data buffer
7			transmit data buffer using	occupies 3K bytes as
3			DMA techniques through a	mentioned above. This
			FIFO buffer in the interface	region is divided into two
₽∭			controller and on to the network." ('094; Col. 1: 60-	1.5K buffers. Only the data that are downloaded to the
$\ \ $			65) (emphasis added).	adapter via bus master
)			(emphasis daded).	transfers are stored in these
1			"Representative prior art	buffers. The controller will
╵║			systems include the	use both the contents of the
2			National Semiconductor	transmit data buffer and the immediate data portion of
			DP83932B, a systems- oriented network interface	the transmit descriptors,
3			controller (SONIC) and the	when encapsulating a frame
.			Intel 82586 local area	for transmission The
4			network coprocessor."	transmit buffers are shared
5			('094; Col. 1: 66 - Col. 2:2).	by the download DMA logic and the transmit DMA
			"The transmit data buffer	logic. The transmit DMA
6			occupies 3K bytes as	logic may switch from
			mentioned above. This	buffer 0 to buffer 1 and back
7			region is divided into two	again freely. The only
Ш			1.5K buffers. Only the data	restriction being the

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
		that are downloaded to the	availability of transmit data
		adapter via bus master	as defined by the transmit
		transfers are stored in these	start threshold register. The
		buffers. The controller will	transmit DMA module
		use both the contents of the	switches from one buffer to the other whenever it has
		transmit data buffer and the immediate data portion of	completed a transmission.
		the transmit descriptors,	The buffer switch occurs
		when encapsulating a frame	regardless of whether or not
		for transmission. The	the transmission was
		adapter automatically	successful and regardless of
		alternates the use of the	whether or not bus master
		buffers after choosing the	download data were used in
		buffer closest to the base of	the preceding transmission.
		the memory as the power up	")
		default." ('094; Col. 12: 45-	
		53) (emphasis added).	<u>DICTIONARY/TREATISE</u> <u>DEFINITIONS</u> :
		"The <i>transmit buffers</i> are	<u> </u>
		shared by the download	The Network Interface
		DMA logic and the transmit	Technical Guide, (First
		DMA logic. The transmit	Edition, 1992)
		DMA logic may switch	Buffer: A temporary storage
		from buffer 0 to buffer 1	area in random access
		and back again freely. The	memory where the NIC or
		only restriction being the	computer stores information
		availability of transmit data	(usually while transmitting or receiving network
		as defined by the transmit start threshold register. The	traffic).
		transmit DMA module	uume).
		switches from one buffer to	EXPERT TESTIMONY:
		the other whenever it has	
		completed a transmission.	Realtek's expert, Dr. Izhak
		The buffer switch occurs	Rubin, may provide
		regardless of whether or not	testimony as to the
		the transmission was	definition of the disputed
		successful and regardless of	terms as would be
		whether or not bus master	understood by one of
		download data were used in	ordinary skill in the relevant
		the preceding transmission."	art and may provide an
		('094; Col. 12: 54-63)	explanation of the technology.
		(emphasis added).	weimorogy.
		"The download DMA	PRIOR ART:
		module may only switch	
		from one <i>buffer</i> to the other,	Datesheet for "82596CA
		if the <i>buffer</i> it is going to	High-Performance 32-Bit
		switch to is not being used	Local Area Network
		by the transmit DMA	Coprocessor," November
		module. Download DMA	1989, Intel Corp, pg. 2
		will attempt to switch from	("Two large, independent
		1	EIEO 1001 / C
		one <i>buffer</i> to another every time it completes processing	FIFOs-128 bytes for Receive and 64 bytes for

### Case3:03-cv-02177-VRW Document303 Filed01/18/06 Page87 of 195

disputed terms in bold)  construction and supporting evidence  of a transmit descriptor as described below. regardless of whether or not any bus master operations were called for in the preceding described below. Figure 1 and the state of the support of the sup	_				
evidence  or of a transmit descriptor as described below, regardless of whether or not any bus master operations were called for in the preceding descriptor. However, it will not change to a buffer that is in use by the transmit DAM module." (1994; Col. 12. 64 - Col. 13: 5) (emphasis added.)  The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffer saler choosing the buffer for the size of the buffers after choosing the buffer saler choosing the buffer for the size of the buffers after choosing the buffer saler choosing the buffer saler in the sea of the buffers after choosing the buffer for the size of the buffer saler in the sea of the sea of the s	1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
of a transmit descriptor as described below, regardless of whether or not any bus master operations were called for in the preceding descriptor. However, it will not change to a buffer that is in use by the transmit DMA module." ('094; Col. 12: 64 - Col.13: 5) (emphasis added).  The rransmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5k buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the transmit data buffer and the immediate data protino of the output data stream to compensate for delays involved in accessing the buffer memory.")  18  19  20  21  22  23  24  25  26  During prosecution of the application that issued as the 872 patent, in a Response dated rebrausy 23, 1994, 3Com stated the following.  "Accordingly, the Fifoy for transferring data to/from the system interface and final for the network." The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network and the network. The FIFOs provides the network and the network and the network and the	2	(disputed terms in <b>bold</b> )		11 0	
described below, regardless of whether or not any bus master operations were called for in the preceding descriptor. However, it will not change to a buffer that is in use by the transmit DMA module." (1994, Col. 12: 64 - Col.13: 5) (emphasis added).  8			evidence		
master operations were called for in the preceding descriptor. However, it will not change to a buffer that is in use by the transmit DMA module." (1994; Col. 12: 64 - Col. 12: 65 (remphasis added).  8	3				latencies and provide
called for in the preceding descriptor. However, it will not change to a buffer that is in use by the transmit DMA module." ('094; Col. 12: 64 - Col.13: 5) (emphasis added).  "The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5k buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the transmit data puffer cosests to the base of the memory as the power up default." ('459; Col. 13: 59-68) (emphasis added).  PROSECUTION HISTORY:  The following citation to the prosecution history of the parent '872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following: "Accordingly, the Firoorymand, et al. reference does not initiate  The FIPO provides  The FIPO provides  The FIPO provides  The FIPO provides  The FIPO provides  The FIPO provides  The FIPO provides  The FIPO provides					
descriptor. However, it will not change to a huffer that is in use by the transmit DMA module." (194; Col. 12: 64 - Col. 13: 65) (remphasis added).  8	4				
not change to a buffer that is in use by the transmit DMA module." ('094; Col. 12: 64 - Col.13: 5) (emphasis added).  10  10  11  10  11  11  11  12  13  11  14  15  16  17  18  18  19  19  10  10  10  11  11  11  12  12  13  14  15  16  17  18  18  19  19  10  10  10  10  10  10  11  11	5				
module." (1994; Col. 12: 64 - Col. 13: 5) (emphasis addeed).  "The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5k buffers. Only the data that are downloaded to who adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter and the immediate data portion of the output data attempter. The foreigne Network Data Sealer Pol PROSECUTION HISTORY:  The following citation to the prosecution history of the parent '872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the "872 patent, in a Response dated February 23, 1994, 3Com stated the following."  The FIFO, provides temporary buffer storage for the provided in the proposed of the provided in the providing a distribution to the real-time demands on the network."  The FIFO provi	3				-
module." (1994, Col. 12: 64 - Col. 13: 59 (emphasis added).  "The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the dapter automatically alternates the use of the buffer altosest to the base of the buffer accessing the buffer obeset to the base of the memory as the power up default." ("459; Col. 13: 59-68) (emphasis added).  PROSECUTION HISTORY:  The following citation to the parent '872 pattent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the 872 pattent, in a Response Stated February 23, 1994, 3 Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate	6			1	
added).  "The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the buffer alter automatically alternates the use of the buffer after choosing the buffer after choosing the buffer after choosing the buffer after chosen to the buffer after chosen to the buffer after chosen to the buffer doses to the base of the memory as the power up default." (*459; Col. 13: 59-68) (emphasis added).  The following citation to the prosecution history of the parent '872 patent supports D-Link's proposed claim construction.  The following citation to the prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate buffer for power buffers. Per provides tendence and form/to the network." The providing tendence and from/to the network. The real-time demands on the network. The FIFO provides tendence and form buffer provides tendence and from the system from the system from the system from the proposed chain construction.					
advanced Micro Devices, Inc., pg. 2-37  "The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffer closest to the base of the buffer closest to the base of the memory as the power up default." ("459; Col. 13: 59-68) (emphasis added).  The following citation to the prosecution history of the parent '872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following:  "Advanced Micro Devices, Inc., pg. 2-37  Inc., pg. 2-37  Inc. pg. pa. pa. poviding a vay to store a portion of the transmitidal parameter for transmission. T	7			, , <u>.</u>	
occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmisson. The adapter automatically alternates the use of the buffer colosest to the base of the buffer colosest to the base of the buffer colosest to the base of the memory as the power up default." (459; Col. 13; 59-68) (emphasis added).  PROSECUTION HISTORY:  The following citation to the prosecution history of the parent "872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the "872 patent, in a Response dated February 23, 1994, 3Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate"  The FIFO provides	o			www.j.	
mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the buffer after choosing the buffer after choosing the buffer safter choosing the buffer closest to the base of the buffer closest to the base of the buffer closest to the base of the buffer safter choosing the buffer closest to the base of the buffer closest to the base of the buffer safter choosing the buffer safter choosing the buffer safter choosing the buffer safter choosing the buffer safter chosing the buffer safter humansision is assured by providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to store a providing a way to s	0				
region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffer closest to the base of the memory as the power up default." ('459, Col. 13: 59- 68) (emphasis added).  PROSECUTION HISTORY:  PROSECUTION HISTORY:  The following citation to the prosecution of the parent '872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following:  The FIFO, providing temporary storage of data, free the host system from the real-time demands on the network.")  Ethernet/IEEE-802.3 Family 1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations  The FIFO provides temporary buffer storage for	9				`
1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffers after choosing the buffers after choosing the buffer closest to the base of the memory as the power up default." ("459; Col. 13: 59-68) (emphasis added).  19  20  21  21  22  21  22  23  24  25  26  During prosecution of the application that issued as the "872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the "872 patent in a Response dated February 23, 1994, 3Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate  127  18					
adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the obligation of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffer closest to the base of the memory as the power up default." ('459; Col. 13: 59-68) (emphasis added).  PROSECUTION HISTORY:  The following citation to the prosecution history of the parent '872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate"  adapter via bus master transfers are stored in these buffer and the immembrated that purporion of the output data stream to compensate for of delays involved in accessing the buffer memory.")  1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp. pg. 1-295:  ("The SONIC incorporates two independent 32-byte FIFOs for transferring data tof/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network.")  Ethernet/IEEE-802.3 Family 1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations  The FIFO provides temporary buffer storage for	10			1.5K buffers. Only the data	temporarily stores data to be
transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the transmit data buffer and the immediate data portion of the output data stream to compensate for delays involved in accessing the buffer after choosing the buffer closest to the base of the buffer closest to the base of the buffer closest to the base of the memory as the power up default." ('459, Col. 13: 59-68) (emphasis added).  PROSECUTION HISTORY:  The following citation to the prosecution history of the parent '872 patent supports D-Link's proposed claim construction.  During prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate"  transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory.")  by 2L ocal Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg. 1-295:  ("The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network." The FIFOs providing temporary storage of data, free the host system from the real-time demands on the network.")  24  25  26  "Accordingly, the Firoozmand, et al. reference does not initiate  The FIFO provides temporary buffer storage for	11				
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24 25 26 27 28 29 29 20 20 20 20 20 20 20 20 20 20 20 20 20				ciaim construction.	
25 26 27 28 27 28 28 29 29 29 29 29 29 29 29 29 29 29 29 29	23			During prosecution of the	the network.")
25 dated February 23, 1994, 3Com stated the following:  1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations")  27 dated February 23, 1994, 3Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate"  The FIFO provides temporary buffer storage for	24				Ethernet/IEEE-802 3 Family
25 26 27 3Com stated the following:  "Accordingly, the Firoozmand, et al. reference does not initiate Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations The FIFO provides temporary buffer storage for					
26 27 "Accordingly, the Firoozmand, et al. reference does not initiate "Accordingly the Firoozmand to all reference temporary buffer storage for the storage for the stor	25				
Firozmand, et al. reference does not initiate  The FIFO provides temporary buffer storage for	26				
does not initiate    The FIFO provides temporary buffer storage for	۷٥				( 1110 Operations
temporary buffer storage for	27				
28	20				temporary buffer storage for

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
2			transmission to the network	data being transferred
3			upon the threshold determination. Rather,	between the parallel bus I/O pins and serial bus I/O pins.
4			transmission to the network	The capacity of the FIFO is
١.			is initiated only when there	48 bytes.
5			is a full frame available in	
			the buffer. When the token	Transmit
6			has been received by the transmitting station, and it	Data is loaded into the FIFO
٦			has a full frame for	under internal micro-
/			transmission, then a	program control.
8			transmission process is	The FIFO must be more
G			begun. The transmission	than 16 bytes empty before
9			process continues, relying on the threshold	the ILACC requests the bus (HOLD/BURREQ is
			determination to keep the	asserted). The ILACC will
10			pipeline full, only while the	start sending the preamble
1 1			token is held by the	(if the line is idle) as soon as
11			transmitting station."	there is one byte loaded into
12			"The environment is substantially different from	the FIFO. Should the transmitter be required to
			the CSMA/CD network,	back off, there will be up to
13			which begins transmission	32 bytes of data in the FIFO
			to the medium access	ready for transmission.
14			controller as soon as the threshold determination is	Reception has priority over transmission during the time
15			met for an incoming frame.	that the transmitter is
13			The MAC may succeed in	backing off.
16			transmitting the frame, may	
			suffer collisions, or may	Receive
17			suffer other types of errors which require backoff.	Data is loaded into the FIFO
18			Thus, the adapter as claimed	from the serial input shift
10			in new claims 24-29,	register during reception
19			initiates transmission	and leaves the FIFO under
			without being assured that the medium access	microprogram control. The ILACC microcode will wait
20			controller is able to gain	until there are at least 16
21			access to the	bytes of data in the FIFO
21			communications medium.	before initiating a DMA
22			This is a much more	burst transfer. Preamble (including the
			sophisticated control environment than that	synchronization bits) is not
23			required by the FDDI	loaded into the FIFO.")
			system of Firoozmand, et	
24			al."	
25			Response dated February 23, 1994, p. 5.	
-3			20, 1771, p. 0.	
26			EXTRINSIC EVIDENCE:	
إر			Drien Ang.	
27			PRIOR ART:	
28		l	l	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence Datesheet for "82596CA	evidence
		High-Performance 32-Bit	
		Local Area Network	
		Coprocessor," November 1989, Intel Corp (Disclosed	
		in D-Link's Preliminary	
		Infringement Contentions),	
		pg. 2:	
		"Two large, independent FIFOs-128 bytes for	
		Receive and 64 bytes for	
		Transmit-tolerate long bus	
		latencies and provide	
		programmable thresholds	
		that allow the user to	
		optimize bus overhead for any worst-case bus latency."	
		any worst-case bus fatelicy.	
		Datasheet for "The	
		SUPERNET 2 Family for	
		FDDI", October 1991,	
		Advanced Micro Devices,	
		Inc. (Disclosed in D-Link's	
		Preliminary Infringement	
		Contentions), pg. 2-37:	
		"The transmit FIFO (Figure 1) is a 36-bit by 9-word	
		first-in-first-out register that	
		temporarily stores data to be	
		transmitted. In this way,	
		continuity of data	
		transmission is assured by	
		providing a way to store a	
		portion of the output data	
		stream to compensate for delays involved in accessing	
		the buffer memory."	
		and control inclinery.	
		1992 Local Area Network	
		<u>Databook Including</u>	
		Datasheet For DP83932B	
		Systems-Oriented Network	
		Interface Controller (SONIC), 1992, National	
		Semiconductor Corp, pg.1-	
		295:	
		"The SONIC incorporates	
		two independent 32-byte	
		FIFOs for transferring data	
		to/from the system interface	
		and from/to the network.	
		The FIFOs, providing	
		temporary storage of data,	1

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
		free the host system from	
		the real-time demands on	
		the network."	
		DICTIONARY/TREATISE	
		DEFINITIONS:	
		McGraw-Hill Illustrated	
		Telecom Dictionary, Fourth Edition, 2001, pg. 83:	
		Buffer - "A temporary	
		storage (memory) device for	
		data. A buffer is basically a	
		box with RAM inside it. A	
		common application for	
		buffers is to collect a stream	
		of data and temporarily	
		store it until another device,	
		such as a PC or server asks	
		the buffer to download it.	
		This is useful when the PC,	
		server or LAN could be out	
		of service for a period of	
		time. When the server or	
		PC is returned to service it just asks for the data from	
		the buffer and it is	
		downloaded. The buffer is	
		then empty and ready to	
		receive more data."	
		Expert Testimony:	
		D-Link's expert, Howard	
		Frazier, may provide	
		testimony as to the	
		definition of the disputed terms as would be	
		understood by one of	
		ordinary skill in the relevant	
		art and may provide an	
		explanation of the	
		technology.	
		D-Link also incorporates by	
		reference Realtek's	
		references.	
"bad frame signal"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
vau ii ailit sigliai			
found in claim	1 - Signar and a manie is odd.		
numbers:	DICTIONARY/TREATISE		
	· ·	contains invalid data.	DICTIONARY/TREATISE
found in claim	A signal that a frame is bad.  DICTIONARY/TREATISE DEFINITIONS:	A specific signal flag indicating that a corresponding frame	a signal indicating the frame is bad.

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
(004 21	evidence	evidence	evidence
'094 patent: 21	See "bad frame signal" in		DEFINITIONS:
-1	subsection 2.		<u>signal</u>
also presented for construction in:	INTERNAL EVIDENCE:		Noveton's' Tologom
construction in.	INTRINSIC EVIDENCE: Claims: claim 25 ("the bad		Newton's' Telecom Dictionary (fourth edition,
'872 patent: 1	frame signal includes a		1991)
_	corrupted error detection		Signal: 1. An electrical
	code"); claim 4; claim 16;		wave used to convey
	claim 21; claim 34; claim		information 2. An alert. 3.
	41; Specification: fig. 18;		An acoustic device (e.g. a
	col. 18:38-41; col. 27:7-9;		bell) or a visual device (e.g.
	col. 27:24-27; col. 27:27-35;		a lamp) which calls
	col. 28:2-5; col. 27: 15-35;		attention. To transmit an
	Fig. 18; see also Prosecution		information signal or
	History: Specification as		alerting signal.
	Filed, p. 53; Specification as		M-C II'II E1 '
	Filed, p. 54; Specification as		McGraw Hill Electronics
	Filed, p. 56; Specification as Filed, p. 57; Specification as		Dictionary (fifth edition, 1994)
	Filed, p. 58; Preliminary		1994)   Signal: Any variation in an
	Amendment, Mar. 3, 1995,		electrical current, visible or
	p. 6; Office Action, Mar. 19,		nonvisible light, audible or
	1996, p. 3; Response to		ultrasonic energy that
	Office Action, Apr. 7, 1997,		conveys information.
	p. 2.		Signals can be coded in
			frequency, phase, or
	EXTRINSIC EVIDENCE:		amplitude to separate them
	3Com's expert, Dr. Michael		from unwanted noise.
	Mitzenmacher may provide		had
	an expert report or other form of testimony regarding		<u>bad</u> :
	the technology to which this		The American Heritage
	term relates and how a		Dictionary of the English
	person having ordinary skill		Language (4th Ed. 2000):
	in the art in the field of		adj. 1. Not achieving an
	networking technology		adequate standard; poor: a
	would understand this term.		bad concert 8. Injuriou
	3Com reserves the right to		in effect; detrimental: bad
	rely on testimony by any		habits. 9. Not working
	expert in this action.		properly; defective: a bad
	Socials IIC Detact No.		telephone connection. 10.
	See also U.S. Patent Nos.		Full of or exhibiting faults
	5,434,872; 5,732,094; 6,327,625; 6,526,446; and		or errors: bad grammar.
	6,570,884; Joint Claim		
	Construction Statement in		INTRINSIC EVIDENCE:
	Cv-05-00098 (VRW).		I THE STOP IN THE
			'872 patent at 28:48-29:2;
	3Com reserves the right to		'094 patent at 27: 15-35
	rely on any statement made		("According to the present
	by any party under the		invention, this transmit data
	Patent Local Rules.		path includes an underrun
			detector 413 for detecting a

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence condition in which the
			transferring of data into the
			transmit data buffer,, b
			the host interface falls
			behind the transferring of
			data into the transmit data
			path 400 by the transmit
			DMA logic The underrun detector
			determines that a transmit
			write TXWR signal is not
			present during an expected
			interval of the frame
			transmission, then a bad
			frame signal is generated o
			line 409")
			'872 patent, Fig. 18; '094
			patent, Fig. 18 ("a signal
			line identified as "bad
			frame" and connected "to
			host interface.")
			EXPERT TESTIMONY:
			Realtek's expert, Dr. Izhak
			Rubin, may provide
			testimony as to the definition
			of the disputed terms as
			would be understood by one of ordinary skill in the
			relevant art and may provid
			an explanation of the
			technology.
"feedback"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION
found in claim	Information from output returned to the input	Information derived from an output to adjust an input.	Information from output that is returned to input
numbers:	Teturned to the input	output to adjust an input.	that is returned to input
	DICTIONARY/TREATISE	REFERENCES:	DICTIONARY/TREATISE
'094 patent: 21, 47	DEFINITIONS: See		DEFINITIONS:
alaa muaaanta difan	"feedback" in subsection 2.	PATENT SPECIFICATION:	Webster's Ninth New
also presented for construction in:	INTRINSIC EVIDENCE:	The following citations support D-Link's proposed	Collegiate Dictionary (nint
	Claims: see, e.g., claim 51	claim construction.	edition, 1988)
'872 patent: 10	("the step of altering the		Feedback: 1. the return to
	threshold value includes	"The transmit logic 39 also	the input of a part of the
	using a driver in the host	supplies status information	output of a machine, system
	system to process the status	across line 44 to the host	or process (as for producing
	information, and in response write a new threshold value	interface logic 31, for posting to the host system.	changes in an electronic circuit that improve
	in a register on the network	The status information	performance or in an
	interface device"); see also	includes indications of	automatic control device
	claim 8; claim 13; claim 21;	underrun conditions and	that provide self-corrective

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supportin
	evidence	evidence	evidence
	claim 31; claim 46; claim	may be used by the host to	action.)
	47; Specification: see, e.g.,	optimize the value in the	
	figs. 2, 4, 13, 14, 17, 18; col.	threshold store 43." ('094;	The American Heritage
	2:24-27 ("the threshold	Col. 4: 47-51) (emphasis	Dictionary of the English
	value may be set by the host	added).	Language (4th ed. 2000)
	system to optimize	(GE) 1 C (1: '.	The return of a portion of
	performance using the alterable threshold store and	"The value for this register	the output of a process or
		may be programmed by the	system to the input,
	the posted status information"); see also Col.	host to optimize	especially when used to maintain performance or to
	2: 21-26; Col. 18: 20-41;	performance. If set too low, system latencies or	control a system or process
	Col. 14: 6-9; Col. 28: 1-17;	bandwidth limitations may	control a system of process
	Col. 4: 47-51; see also	cause the adapter to	IBM Dictionary of
	Prosecution History:	underrun the network during	Computing (10th ed. 1993)
	Specification as Filed, p. 55;	transmission, causing a	The return of part of the
	Specification as Filed, p. 58;	partial frame with a	output of a machine,
	Preliminary Amendment,	guaranteed bad CRC to be	process, or system as input
	Mar. 3, 1995, p. 6; Office	transmitted. If the value is	to the computer, especially
	Action, Mar. 19, 1996, p. 4;	set too high, then	for self-correcting or contr
	Response to Office Action,	unnecessary delays will be	purposes.
	Apr. 7, 1997, p. 2.	incurred before the start of	-
		transmission. The adapter	Microsoft Computer
	EXTRINSIC EVIDENCE:	generates an indication of an	Dictionary (5th ed. 2002):
	3Com's expert, Dr. Michael	underrun condition which is	The return of a portion of
	Mitzenmacher may provide	made available to the host	system output as input to the
	an expert report or other	through the XMIT	same system
	form of testimony regarding	FAILURE register. If such	Newton's' Telecom
	the technology to which this	an underrun indication	Dictionary (fourth edition,
	term relates and how a	occurs, then the host driver	1991)
	person having ordinary skill in the art in the field of	should increase the value on	Feedback: The return of pa
	networking technology	the XMIT START	of an output signal back to the input side of the device
	would understand this term.	THRESH register. Further underrun indications should	Think of the high-pitched
	3Com reserves the right to	cause the driver to	squeal you hear when
	rely on testimony by any	continually increase the	someone brings a
	expert in this action.	XMIT START THRESH	microphone too close to th
	expert in this detion.	value. If the XMIT START	loudspeaker. Not all
	See also U.S. Patent Nos.	THRESH value is increased	feedback is as obvious or a
	5,434,872; 5,732,094;	to a value of greater than the	irritating. Some feedback i
	6,327,625; 6,526,446; and	maximum length expected	good.
	6,570,884; Joint Claim	by the system, then the early	
	Construction Statement in	transmit start features	Newton's Telecom
	Cv-05-00098 (VRW).	should be disabled by	Dictionary (17th ed. 2001)
		writing a zero to the XMIT	The return of part of an
	3Com reserves the right to	START THRESH register."	output signal back to the
	rely on any statement made	('094; Col. 28: 1-17).	input side of the device.
	by any party under the		
	Patent Local Rules.	"The XMIT FAILURE	EXPERT TESTIMONY:
		field contains the error code	
		that is made up of the status	Realtek's expert, Dr. Izhak
		bits gathered from the	Rubin, may provide
		Ethernet transmitter after	testimony as to the
	1	İ	definition of the disputed

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1	Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
2		evidence	evidence	evidence
3			the completion of transmission. This field is	terms as would be understood by one of
			mapped to the XMIT	ordinary skill in the relevant
4			FAILURE register for host	art and may provide an explanation of the
5			access." ('094; Col. 14: 6-9).	technology.
			7).	
6			"XMIT FAILURE returns	
7			the cause of a transmit failure. This register returns	
			the cause of the failure of	
8			the attempt(s) to transmit a	
9			queued frame. A non-zero value indicates that the	
9			frame encountered one or	
10			more errors during the	
,,			transmission attempt. The bits in this register are	
11			defined as follows: bit 0	
12			DMA UNDERRUN This register will contain	
			valid data regardless of the	
13			success or failure of the	
14			attempt to transmit a frame.	
			If there was no failure, then this register will contain a	
15			value of 0 (hex). The	
16			contents of this register are valid after the frame has	
10			completed transmission	
17			(low byte of XMIT FRAME	
18			STATUS not equal to ff (hex)) and before XMIT	
10			PROT ID is read. If a data	
19			underrun occurs, the adapter	
20			will force a CRC error into the frame during	
۷٠			transmission to assure that	
21			the frame is received as a bad frame and is discarded	
22			by the destination device."	
22			('094; Col. 18: 20-41).	
23			"In one aspect of the	
24			invention, the monitoring	
24			logic includes a threshold	
25			store, which is programmable by the host	
			computer for storing a	
26			threshold value and logic for	
27			posting status information to the host. Thus, the	
	L	I	and nost. Thus, the	

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
	eviaence	threshold value may be set	eviaence
		by the host system to	
		optimize performance using	
		the alterable threshold store	
		and the posted status	
		information." ('094; Col. 2:	
		21-26).	
		PROSECUTION HISTORY:	
		Claim 10 of the parent	
		'872 patent was amended to	
		show feedback for use by	
		the host system: "	
		control means, coupled with the network interface	
		means, for posting status	
		information [which may be	
		used] <u>for use</u> by the host	
		system, as feedback for	
		optimizing the threshold	
		value." ('872 prosecution	
		history, Response mailed February 23, 1994, p. 2).	
		1 Columny 23, 1794, p. 2).	
		EXTRINSIC EVIDENCE:	
		DICTIONARY/TREATISE	
		DEFINITIONS:	
		Newton's Telecom	
		<u>Dictionary</u> , 19 <sup>th</sup> Ed., 2003,	
		pg. 319: Feedback - "The return of	
		part of an output signal back	
		to the input side of the	
		device."	
		Webster's Ninth New	
		Collegiate Dictionary,	
		(1986), pg. 454:	
		Feedback - "The return to	
		the input of a part of the	
		output of a machine, system, or process (as for producing	
		changes in an electronic	
		circuit that improve	
		performance or in an	
		automatic control device	
		that provide self-corrective	
		action)."	

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supportin
	evidence	evidence EXPERT TESTIMONY:	evidence
		D-Link's expert, Howard Frazier, may provide	
		testimony as to the definition of the disputed terms as would be	
		understood by one of ordinary skill in the relevant art and may provide an	
		explanation of the technology.	
"host system"	PROPOSED CONSTRUCTION: A computer that	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
found in claim numbers:	communicates over a network	Any system or computer that communicates over a network	Any system or computer that communicates over a network
'094 patent: 1, 9, 21, 28, 39, 47	DICTIONARY/TREATISE DEFINITIONS: Webster's New	Evidence	Evidence
also presented for construction in:	World Computer Dictionary (10th ed. 2003): 1. In the Internet, any computer that	(872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62)	(872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62)
'459 patent: 1	can function as the beginning and end point of	Furthermore, the prior art systems which use transmit data buffers require the <i>host</i>	Furthermore, the prior art systems which use transmidata buffers require the <i>ho</i>
'872 patent: 1, 10, 21	data transfers. An Internet host has a unique Internet	or sending system to manage the transmit data	or sending system to manage the transmit data
'884 patent: 1	address (called an IP address) and a unique domain name. 2. In	buffer. (872: Col. 3, ln. 65 to col.	buffer. (872: Col. 3, ln. 65 to col.
	networks and telecommunications	4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1,	4., ln. 2) ('094: Col. 3, lns 59-64) As shown in FIG.
	generally, a server that performs centralized functions, such as making	such system for communicating data	such system for communicating data
	program or data files available to other	includes a host data processing system, generally referred to by	includes a host data processing system, generally referred to by
	computers; The American Heritage Dictionary of the	reference number 1, which includes a host system bus	reference number 1, which includes a host system bus
	English Language (4th ed. 2000): Computer Science. A computer containing data or	2, a host central processing unit 3, host memory 4, and other host devices 5, all	2, a host central processing unit 3, host memory 4, and other host devices 5, all
	programs that another computer can access by	communicating across the bus 2	communicating across the bus 2
	means of a network or modem; <u>Dictionary of</u>		
	Computing (3d ed. 1990): Host computer (host): A computer that is attached to	(884: Col. 2, lns. 39-44) The invention is particularly suited to environments in	(884: Col. 2, lns. 39-44) The invention is particular suited to environments in
	a network and provides services other than simply	which the host system is actively handling	which the host system is actively handling
	acting as a store-and-	communications and other	communications and other

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
	forward processor or	processing tasks, and in	processing tasks, and in
	communication switch.	which the adapter is able to	which the adapter is able to
		take over some specialized	take over some specialized
	INTRINSIC EVIDENCE:	tasks without interfering	tasks without interfering
	Claims claim 1; claim 8;	with the active processing in	with the active processing in
	claim 9; claim 11; claim 12;	the host system.	the host system.
	claim 13; claim 17; claim		
	21; claim 22; claim 26; claim 28; claim 29; claim		
	30; claim 31; claim 35;		
	claim 39; claim 46; claim		
	47; claim 51; Specification:		
	see, e.g., col. 4:2-5 ("The		
	network adapter 6 is, in		
	turn, connected to an		
	adapter memory 9, which is		
	managed by the interface controller 6 or by the host		
	CPU3"); see also col. 1:60-		
	62; col. 1:45-48; col. 1:53-		
	55; col. 1:57-59; col. 1:59-		
	63; col. 2:9-11; col. 2:11-15;		
	col. 2:20-23; col. 2:23-27;		
	col. 2:29-31; col. 2:46-52;		
	col. 2:63-1; col. 3:5-8; col. 3:8-10; col. 3:10-12; col.		
	3:55-64; col. 4:5-8; col. 4:8-		
	10; col. 4:13-14; col. 4:18-		
	21; col. 4:21-23; col. 4:23-		
	25; col. 4:25-27; col. 4:38-		
	39; col. 4:39-41; col. 4:47-		
	49; col. 4:49-52; col. 4:52-		
	53; col. 4:53-55; col. 4:55- 57; col. 4-5:53-4; col. 5:4-9;		
	col. 5:9-13; col. 5:18-21;		
	col. 5:21-23; col. 5:23-26;		
	col. 5:39-42; col. 5:45-47;		
	col. 5:50-52; col. 6:12-14;		
	col. 6:20-22; col. 6:34-36;		
	col. 6-7:67-3; col. 7:39-43;		
	col. 7:43-47; col. 7:51-53; col. 7:54-59; col. 8:4-5; col.		
	8:18-22; col. 8:30-32; col.		
	8:38-43; col. 9:38-41; col.		
	9:41-47; col. 9:50-52; col.		
	9:59-63; col. 9:63-66; col.		
	9-10:66-3; col. 10:3-6; col.		
	10:11-13; col. 10:27-30; col.		
	11:8-12; col. 11:12-14; col.		
	11:14-15; col. 11:15-18; col. 11:18-19; col. 11:19-21; col.		
	11:27-31; col. 11:31-34; col.		
		1	1

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
3		11:46-52; col. 11:52-53; col. 11:53-57; col. 11:62-66; col.		
3		11-12:66-1; col. 12:1-2; col.		
4		12:2-4; col. 12:10-11; col.		
.		12:18-21; col. 12:21-24; col.		
5		12:24-29; col. 12:29-30; col.		
		13:14-17; col. 13:22-26; col.		
6		13:26-28; col. 13:51-54; col. 13:57-61; col. 14:2-6; col.		
٦		14:8-10; col. 14:14-16; col.		
7		14:16-18; col. 14:18-21; col.		
8		14:27-30; col. 14:36-37; col.		
		14:37-42; col. 14:42-43; col.		
9		14:43-45; col. 14:45-48; col. 14:51-53; col. 14:53-56; col.		
		14:58-60; col. 14:62-64; col.		
10		15:8-10; col. 15:10-13; col.		
		15:16-18; col. 15:20-21; col.		
11		15:24-27; col. 15:27-28; col.		
12		15:28-36; col. 15:38-41; col.		
12		15:42-45; col. 15:45-47; col. 15:48-53; col. 15:64-1; col.		
13		16:1-2; col. 16:2-5; col.		
		16:5-7; col. 16:7-11; col.		
14		16:11-14; col. 16:25-30; col.		
1.5		16:44-49; col. 16:49-51; col.		
15		16:51-56; col. 16:59-63; col. 16-17:66-1; col. 17:10-11;		
16		col. 17:15-18; col. 17:27-30;		
		col. 17:30-34; col. 17:48-51;		
17		col. 17:53-55; col. 17:59-63;		
4.0		col. 18:10-12; col. 18:54-58; col. 19:14-17; col. 19:38-41;		
18		col. 19:61-64; col. 19-		
19		20:67-1; col. 20:5-9; col.		
17		20:19-22; col. 20:46-47; col.		
20		20:47-51; col. 20:58-60; col. 20:60-63; col. 20:63-67; col.		
		20:60-63; col. 20:63-67; col. 21:7-10; col. 21:10-11; col.		
21		21:22-28; col. 21:28-29; col.		
22		21:29-33; col. 21:33-34; col.		
22		21:53-55; col. 21:55-58; col.		
23		22:5-6; col. 23:33-38; col. 24:8-12; col. 24:27-30; col.		
		24:31-39; col. 24:54-55; col.		
24		25:39-43; col. 26:7-9; col.		
_		27:16-21; col. 28:1-2; col.		
25		28:7-9; col. 28:9-11; <u>see</u>		
26		also Prosecution History: Specification as Filed, p. 52;		
۷٥		Specification as Filed, p. 52; Specification as Filed, p. 52;		
27		Specification as Filed, p. 55;		
		Specification as Filed, p. 55;		
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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting evidence	construction and supporting evidence
	evidence	eviaence	evidence
	Specification as Filed, p. 56;		
	Specification as Filed, p. 57;		
	Specification as Filed, p. 58;		
	Preliminary Amendment,		
	Mar. 3, 1995, p. 2;		
	Preliminary Amendment,		
	Mar. 3, 1995, p. 2; Preliminary Amendment,		
	Mar. 3, 1995, p. 6; Office		
	Action, Mar. 19, 1996, p. 2;		
	Office Action, Mar. 19,		
	1996, p. 2; Office Action,		
	Mar. 19, 1996, p. 2; Office		
	Action, Mar. 19, 1996, pp.		
	2-3; Office Action, Mar. 19,		
	1996, p. 3; Office Action,		
	Mar. 19, 1996, p. 4; Office		
	Action, Mar. 19, 1996, p. 4;		
	Office Action, Mar. 19,		
	1996, p. 4; Office Action,		
	Mar. 19, 1996, p. 5; Office		
	Action, Mar. 19, 1996, p. 6;		
	Office Action, Mar. 19,		
	1996, pp. 6-7; Office		
	Action, Mar. 19, 1996, p. 7;		
	Office Action, Mar. 19,		
	1996, p. 7; Office Action,		
	Mar. 19, 1996, p. 8; Office		
	Action, Mar. 19, 1996, p. 8;		
	Office Action, Jan. 7, 1997,		
	p. 2; Response to Office		
	Action, Apr. 7, 1997, pp. 1-		
	2; Response to Office		
	Action, Apr. 7, 1997, p. 2;		
	Response to Office Action,		
	Apr. 7, 1997, p. 5; Response		
	to Office Action, Apr. 7,		
	1997, p. 5; Response to		
	Office Action, Apr. 7, 1997,		
	p. 5; Response to Office		
	Action, Apr. 7, 1997, p. 5;		
	Response to Office Action,		
	Apr. 7, 1997, p. 5; Response		
	to Office Action, Apr. 7,		
	1997, p. 5		
	EXTRINSIC EVIDENCE:		
	3Com's expert, Dr. Michael		
	Mitzenmacher may provide		
	an expert report or other		
	form of testimony regarding		
	the technology to which this		
	term relates and how a		

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	D-Link's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
	person having ordinary skill in the art in the field of		
	networking technology would understand this term.		
	3Com reserves the right to rely on testimony by any expert in this action.		
	See also U.S. Patent Nos.		
	5,434,872; 5,732,094; 6,327,625; 6,526,446; and		
	6,570,884; Joint Claim Construction Statement in		
	Cv-05-00098 (VRW).		
	3Com reserves the right to rely on any statement made by any party under the		
( 4 · · · ·	Patent Local Rules.	Proposition government	Proposer governversov
"optimizing the threshold"	PROPOSED CONSTRUCTION: Attempting to make the transmission of frames more	PROPOSED CONSTRUCTION: Adjusting the current threshold amount to make it	PROPOSED CONSTRUCTION: Dynamically changing the threshold value by the host
found in claim numbers:	efficient.	as efficient, effective, or functional as possible.	system to make it as perfect effective, or functional as
'094 patent: 21	DICTIONARY/TREATISE DEFINITIONS: See "optimizing the	REFERENCES:	possible.  Intrinsic Evidence:
also presented for construction in:	threshold" in subsection 2.	EXTRINSIC EVIDENCE:	'872 patent, Abstract; '094
'872 patent: 10	INTRINSIC EVIDENCE: Claims see claim 8; claim	DICTIONARY/TREATISE DEFINITIONS:	patent, Abstract ("The monitoring logic includes <i>a</i>
	13; claim 21; claim 31; claim 46; claim 48; Specification: see, e.g., figs.	Webster's II New College Dictionary (1999):	threshold store, which is programmable by the host
	2, 4, 13, 14, 17, 18; col. 2:24-27 ("the threshold	optimize: 1. To improve or develop as far as possible.	computer for storing a threshold value. Thus, the threshold value may be set
	value may be set by the host system to optimize	2. To make the most effective use of.	by the host system to optimize performance in a
	performance using the alterable threshold store and	WordNet 2.1 lexical	given setting.")
	the posted status information"); col. 4:38-41; col. 4:49-51; col. 28:1-2;	database, Princeton Univ. (1991-2005) at http://wordnet.princeton.edu	'872 patent at 2:27-34; '094 patent at 2: 21-27 ("In one aspect of the invention, the
	col. 27:65-67; col. 4:38-46; col. 2: 21-27; col. 27:44-	/perl/webwn make optimal; get the most	monitoring logic includes <i>a</i> threshold store, which is
	28:-17; see also Prosecution History:	out of; use best - 'optimize your resources'; modify to	programmable by the host computer for storing a
	Specification as Filed, p. 55; Specification as Filed, p. 58;	achieve maximum efficiency in storage	threshold value and logic for posting status
	Preliminary Amendment, Mar. 3, 1995, p. 6; Office	capacity or time or cost - 'optimize a computer	information to the host. Thus, the threshold value
	Action, Mar. 19, 1996, p. 4; Response to Office Action,	program'''	may be set by the host system to optimize

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
		Apr. 7, 1997, p. 2.	EXPERT TESTIMONY:	performance using the
3		Evennique Evennues.	D Link's sum out Housend	alterable threshold store
4		EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael	D-Link's expert, Howard Frazier, may provide	and the posted status information.")
		Mitzenmacher may provide	testimony as to the	·
5		an expert report or other form of testimony regarding	definition of the disputed terms as would be	'872 patent at 4:46-55; '094 patent at 4:38-46 ("The
6		the technology to which this	understood by one of	threshold store 43, in a
		term relates and how a	ordinary skill in the relevant	preferred system, is
7		person having ordinary skill in the art in the field of	art and may provide an explanation of the	dynamically programmable by the host computer 30. In
8		networking technology	technology.	this embodiment, the
		would understand this term.  3Com reserves the right to	D-Link also incorporates by	threshold store 43 is a register accessible by the
9		rely on testimony by any	reference Realtek's	host through the interface
10		expert in this action.	references.	logic 31. Alternatively, the
		See also U.S. Patent Nos.		threshold store may be a read only memory set during
11		5,434,872; 5,732,094;		manufacture. In yet other
12		6,327,625; 6,526,446; and 6,570,884; Joint Claim		alternatives, the threshold store <i>may be implemented</i>
		Construction Statement in		using user specified data in
13		Cv-05-00098 (VRW).		non-volatile memory, such
14		3Com reserves the right to		as EEPROMs, FLASH EPROMs, or other memory
		rely on any statement made		storage devices.")
15		by any party under the Patent Local Rules.		'872 patent at 29:12-57;
16		Tatent Local Rules.		'094 patent at 27:44-28:-17
				("XMIT START THRESH
17				is used to specify the number of bytes of the
18				transmit frame that must
				reside on the adapter,, before the adapter can
19				commence with the media
20				access control functions
				associated with transmitting the frame.
21				
22				The value for this register may be programmed by the
22				host to optimize
23				performance The adapter generates an
24				indication of an underrun
25				condition which is made
25				available to the host through the XMIT FAILURE
26				register. If such an underrun
27				indication occurs, then the host driver should increase
27				the value on the XMIT
28				the value on the XMIT

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1	Cl.: 1	20	D. I 12	D 1 . 1 2 1
1	Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
2	(	evidence	evidence	evidence
3				START THRESH register. Further underrun indications
4				should cause the driver to continually increase the
5				XMIT START THRESH value ")
6				DICTIONARY/TREATISE DEFINITIONS:
7				See "altering the threshold" for definitions
8				of "threshold."
9				Optimize:
10				Webster's Ninth New Collegiate Dictionary, (ninth edition, 1988)
11				Optimize: to make as
12				perfect, effective, or functional as possible.
13				EXPERT TESTIMONY:
14				Realtek's expert, Dr. Izhak
15				Rubin, may provide testimony as to the
16				definition of the disputed terms as would be
17				understood by one of ordinary skill in the relevant
18				art and may provide an explanation of the technology.
19	"threshold amount of	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
20	data"	A value representing the quantity of data sufficient to	The amount of data required for some process to take	The amount of data required for some process to take
21	found in claim numbers:	trigger the initiation of transmission	place.	place.
22	'094 patent: 21	DICTIONARY/TREATISE	REFERENCES:	Digition and The Attice
23		DEFINITIONS: See "threshold value" in subsection 1 for definitions	PATENT SPECIFICATION:	DICTIONARY/TREATISE DEFINITIONS: threshold
24		of "threshold" and "data	The following citations	
25		value" in subsection 6 for definitions of "data."	support D-Link's proposed claim construction.	The American Heritage Dictionary of the English Language (4th ed. 2000):
26		INTRINSIC EVIDENCE: Claims: claim 7; claim 8;	"Coupled with the <i>threshold</i> logic 36 is a	The point that must be exceeded to begin
27		claim 9; claim 10; claim 12; claim 13; claim 15; claim	threshold store 43 which stores a threshold value	producing a given effect or result or to elicit a response.
28		1 , , , , , , , , , , , , , , , , , , ,	100	

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence	evidence	evidence
2		21; claim 22; claim 23; claim 28; claim 30; claim	which indicates an amount of data of a frame that must	McGray, Hill Floatranias
3		31; claim 32; claim 45;	be resident in the frame	McGraw-Hill Electronics Dictionary (fifth edition,
4		claim 46; claim 47; claim	buffer 34 before	1994)
7		48; claim 49; claim 50;	transmission of that frame	Threshold: 1. The least
5		claim 51; claim 53;	may be initiated by the	value of a current, voltage,
		Specification: see, e.g., figs.	transmit DMA logic and	or other quantity that
6		11-17; col. 2:15-21 ("The	MAC 39." ('094; Col. 4:	produces the minimum
		network interface controller	32-37) (emphasis added).	detectable response. It is also called a limen. 2. The
7		includes logic for initiating transmission of the frame	"When the <i>threshold</i>	level of pumping at which a
		when the threshold	amount of data is resident in	laser can go into self-excited
8		determination indicates that	the buffer 34, then the	oscillation.
9		a sufficient portion of the	transmit logic 39 is	
7		frame is resident in the	instructed to begin	threshold value
10		transmit buffer, and prior to	transmission of the frame.	MaCross IIII Flori
- 7		the transfer of all of the data of the frame into the	The transmit logic 39 then begins retrieving data from	McGraw-Hill Electronics Dictionary (fifth edition,
11		transmit buffer"); see also	the buffer 34 to support	1994)
		col. 2:10-12; col. 2:20-26;	transmission of the frame on	Threshold Value: The
12		col. 2:39-43; col. 2:41-45;	the medium 42. This	minimum input that
1.0		col. 3:26-29; col. 3:50-52;	operation begins before the	produces a corrective action
13		col. 4:8-11; col. 4:23-33;	entire frame has been	in an automatic control
14		col. 4:38-46; col. 4:49-51; col. 4:57-61; col. 4:53-5:3;	transferred from the host computer 30 into the buffer	system.
17		col. 12:57-58; col. 18:10-12;	34, if the transmit logic 39	EXPERT TESTIMONY:
15		col. 21:3-4; col. 23:33-37;	is available to transmit the	
		col. 23:45-49; col. 23:58-69;	frame subject of the ongoing	Realtek's expert, Dr. Izhak
16		col. 24:1-3; col. 24:52-54;	download from the host	Rubin, may provide
		col. 25:53-55; col. 27:57-63; col. 2: 40-46; col. 20: 10-36;	computer 30, the frame	testimony as to the definition of the disputed
17		FIG. 1; col. 4: 59- 5: 3; col.	being downloaded into the buffer 34 is larger than the	terms as would be
18		4: 32-37; col. 3:54-59; see	threshold set by the	understood by one of
10		also Prosecution History:	threshold store 43, and the	ordinary skill in the relevant
19		Specification as Filed, p. 52;	host computer 30 indicates	art and may provide an
17		Specification as Filed, p. 53;	that immediate transmission	explanation of the
20		Specification as Filed, p. 55; Specification as Filed, p. 56;	of the data is desired."	technology.
		Specification as Filed, p. 57;	('094; Col. 4: 59-Col. 5: 3) (emphasis added).	
21		Specification as Filed, p. 58;	(Timpinoso addou).	
22		Preliminary Amendment,	"FIG. 1 illustrates a data	
22		Mar. 3, 1995, p. 6; Office	communication system	
23		Action, Mar. 19, 1996, p. 4;	according to the present	
23		Office Action, Mar. 19, 1996, pp. 6-7; Office	invention with a controller circuit using a dedicated	
24		Action, Mar. 19, 1996, pp.	transmit buffer memory	
		7-8; Response to Office	which is automatically	
25		Action, Apr. 7, 1997, p. 2.	enabled to begin	
اء			transmission of a frame on	
26		EXTRINSIC EVIDENCE:	the network when the	
27		3Com's expert, Dr. Michael Mitzenmacher may provide	number of bytes available in the transmit buffer memory	
27		an expert report or other	exceeds a preprogrammed	
28	L	r · · · · · · · · · · · · · · · · · · ·		
-0				

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supportin
	evidence	evidence	evidence
	form of testimony regarding the technology to which this	threshold." ('094; Col. 3: 54-59) (emphasis added).	
	term relates and how a	54-57) (cimpilasis added).	
	person having ordinary skill	"XMIT START THRESH	
	in the art in the field of	provides for an early start of	
	networking technology	transmission. The XMIT	
	would understand this term.	START THRESH register is	
	3Com reserves the right to	used to specify the number	
	rely on testimony by any	of transmit bytes that must	
	expert in this action.	reside on the adapter before it will start transmission.	
	See also U.S. Patent Nos.	Values greater than the	
	5,434,872; 5,732,094;	maximum frame length will	
	6,327,625; 6,526,446; and	prevent this function from	
	6,570,884; Joint Claim	operating properly. The	
	Construction Statement in	method for disabling this	
	Cv-05-00098 (VRW).	function is to set the register	
	2Com magamus 41 1.4	to zero. Bytes are counted	
	3Com reserves the right to	starting with the first byte of the destination field of the	
	rely on any statement made by any party under the	transmit frame. The number	
	Patent Local Rules.	of bytes considered to be	
	Tutont Booti Ruies.	available is the sum of the	
		immediate data written to	
		XMIT AREA by the host	
		and those bytes transferred	
		to the transmit data buffers	
		in the adapter using bus	
		master DMA operations.	
		The transmit request will be posted immediately after	
		XMIT START THRESH	
		transmit frame bytes are	
		made available from the	
		immediate data or when the	
		adapter has bus-mastered	
		XMIT START THRESH-	
		XMIT IMMED LEN bytes	
		onto the adapter. The number of bytes resident on	
		the adapter must be equal to	
		or greater than the value in	
		XMIT START THRESH	
		for the transmission to	
		commence, unless the total	
		frame size is less than	
		XMIT START THRESH.	
		In that case, the frame will	
		begin transmission when the entire frame has been copied	
		to the adapter. The actual	
		transmission of the frame	
	İ	may be delayed by previous	1

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
1	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2	(anspared terms in every	evidence	evidence	evidence
			pending transmit frames and	
3			by deferrals to network	
4			traffic. This register is set to zero during a reset."	
4			('094; Col. 20: 10-36)	
5			( ,	
			"The threshold logic	
6			determines the amount of	
_			immediate data from the	
7			descriptor, and monitors the downloading of data of the	
8			frame into the download	
0			area. When the	
9			combination meets the	
			threshold, then actual	
10			transmission of the frame is	
			initiated. Thus,	
11			transmission of a frame may be initiated before the	
12			complete frame has been	
12			downloaded into the	
13			download area." ('094; Col.	
			2: 40-46) (emphasis added).	
14			"If host processor 5	
15			responds to network adapter	
13			3 before a complete data	
16			frame is transferred, host	
			processor 5 then may	
17			decrease the <i>threshold value</i> in alterable storage location	
1.0			10a enabling threshold logic	
18			10 to generate the indication	
19			signal at a later time in the	
1)			next transfer of a data frame. Alternatively, if host	
20			processor 5 responds to the	
			network adapter 3 after a	
21			complete data frame has	
22			already been transferred,	
22			host processor 5 may then increase the threshold value	
23			in alterable storage location	
			10a enabling the threshold	
24			logic to generate an	
2.			indication signal at an	
25			earlier time in the next transfer of a data frame."	
26			('459; Col. 6: 48-59)	
20			(emphasis added).	
27				

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
3			EXTRINSIC EVIDENCE:	
4			DICTIONARY/TREATISE DEFINITIONS:	
5			Webster's Ninth New	
6			Collegiate Dictionary (1983), pg.229: Threshold - "A level, point,	
7			or value above which something is true or will	
8			take place and below which it is not or will not."	
9			EXPERT TESTIMONY:	
10 11			D-Link's expert, Howard Frazier, may provide	
12			testimony as to the definition of the disputed terms as would be	
13			understood by one of ordinary skill in the relevant	
14			art and may provide an explanation of the technology.	
15	"underrun"	PROPOSED CONSTRUCTION:	Proposed construction:	PROPOSED CONSTRUCTION:
16	found in claim	When expected data from a frame to be transferred is	The condition of falling behind.	A condition in which the transferring of data into a
17	numbers:	not available	See construction for "falls	transmit data buffer by the host interface falls behind
18	'094 patent: 21 also presented for	DICTIONARY/TREATISE DEFINITIONS: See "underrun" in subsection 2.	behind."	the transferring of data into a transmit data path by a transmit logic.
19	construction in:			
20	'872 patent: 1	INTRINSIC EVIDENCE: Claims: see, e.g., claim 8		INTRINSIC EVIDENCE:
21		("The method as in claim 7, further comprising:		'872 patent at 28:48-29:2 ("According to the present
22		providing access to the threshold value so that it		invention, this transmit data path includes an underrun
23		may be dynamically programmed by the host		detector 413 for detecting a condition in which the
24		system; and posting status information for use by the		transferring of data into the transmit data buffer, or
25		host system as feedback for optimizing the threshold		immediate data to the transmit descriptor buffer,
26		value."); claim 22 ("The method as in claim 21,		by the host interface falls behind the transferring of
27		wherein the threshold amount is dynamically		data into the transmit data path 400 by the transmit
28		programmable by the host		DMA logic The

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
ړ∥	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting evidence
2		evidence computer."); claim 30 ("The	evidence	underrun detector
3		method as in claim 28,		determines that a transmit
ً		wherein the threshold		write TXWR signal is not
4		determination is based on a		present during an expected
.		comparison of the amount		interval of the frame
5		of data transferred into the		transmission, then a bad
		buffer memory with a		frame signal is generated on
6		threshold value, the		line 409 ")
		threshold value being		Every Transition
7		dynamically programmable by the host system."); see		EXPERT TESTIMONY:
		also claim 4; claim 6; claim		Realtek's expert, Dr. Izhak
8		16; claim 20; claim 21;		Rubin, may provide
		claim 34; claim 38; claim		testimony as to the
9		41; claim 44; claim 52;		definition of the disputed
المر		claim 53; Specification: see,		terms as would be
10		<u>e.g.</u> , fig. 18; col. 4:50-52;		understood by one of
11		col. 7:62-4; col. 9:11-13;		ordinary skill in the relevant
. 1		col. 14:22-23; col. 18:26-30;		art and may provide an
12		col. 22:10-12; col. 26:60-61; col. 27:16-21; col. 27:21-23;		explanation of the technology.
		col. 27:25-32; col. 27:34-36;		technology.
3		col. 28:2-5; col. 28:7-17; see		
		also Prosecution History:		
4		Specification as Filed, p. 53;		
		Specification as Filed, p. 54;		
15		Specification as Filed, p. 56;		
ااء		Specification as Filed, p. 57;		
16		Specification as Filed, p. 58; Preliminary Amendment,		
ار.		Mar. 3, 1995, p. 6; Office		
7		Action, Mar. 19, 1996, p. 3;		
8		Response to Office Action,		
. 6		Apr. 7, 1997, p. 2.		
9				
		EXTRINSIC EVIDENCE:		
20		3Com's expert, Dr. Michael		
		Mitzenmacher may provide an expert report or other		
21		form of testimony regarding		
		the technology to which this		
22		term relates and how a		
$\ _{\mathcal{L}_{s}}$		person having ordinary skill		
23		in the art in the field of		
24		networking technology		
-4		would understand this term.  3Com reserves the right to		
25		rely on testimony by any		
		expert in this action.		
26		r		
		See also U.S. Patent Nos.		
27		5,434,872; 5,732,094;		
		6,327,625; 6,526,446; and		

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting	D-Link's proposed construction and supporting	Realtek's proposed construction and supporting
(disputed terms in <b>bota</b> )	evidence	evidence	evidence
	6,570,884; Joint Claim Construction Statement in		
	Cv-05-00098 (VRW).		
	3Com reserves the right to		
	rely on any statement made		
	by any party under the Patent Local Rules.		
"altering the threshold"	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:	PROPOSED CONSTRUCTION:
found in claim	changing	dynamically changing	dynamically changing
numbers:	DICTIONARY/TREATISE DEFINITIONS:	REFERENCES:	INTRINSIC EVIDENCE:
'094 patent: 47	See "alterable storage location" in subsection 1 for	PATENT SPECIFICATION:	'094 patent, Abstract ("The monitoring logic includes a
	definitions of "alter" and	The following citations	threshold store, which is
	"threshold value" in	support D-Link's proposed	programmable by the host
	subsection 1 for definitions of "threshold."	claim construction:	computer for storing a threshold value. Thus, the
	or theshold.	"The threshold store 43, in	threshold value may be set
	<u>Intrinsic evidence:</u>	a preferred system, is	by the host system to
	Claims: see, e.g., claim 49	dynamically programmable	optimize performance in a
	("including allowing alteration of the threshold	by the host computer 30. In this embodiment, the	given setting.")
	value while data of a frame	threshold store 43 is a	'094 patent at 4:38-46 ("The
	to be transmitted is stored in	register accessible by the	threshold store 43, in a
	the buffer memory"); see also claim 47; claim 48;	host through the interface logic 31." ('094; Col. 4: 38-	preferred system, is dynamically programmable
	claim 50; claim 51; claim	41).	by the host computer 30. In
	53; <u>Specification</u> : <u>see, e.g.</u> ,	%T11 C4	this embodiment, the threshold store 43 is a
	figs. 2, 4, 13, 14, 17, 18; col. 4:38-39 ("The threshold	"The value for this register may be programmed by the	register accessible by the
	store 43, in a preferred	host to optimize	host through the interface
	system, is dynamically	performance. If set too low,	logic 31. Alternatively, the
	programmable by the host computer 30"); col. 4:43-46	system latencies or bandwidth limitations may	threshold store may be a read only memory set
	("In yet other alternatives,	cause the adapter to	during manufacture. In yet
	the threshold store may be	underrun the network during	other alternatives, the threshold store may be
	implemented using user specified data in non-	transmission, causing a partial frame with a	implemented using user
	volatile memory, such as	guaranteed bad CRC to be	specified data in non-
	EEPROMs, FLASH	transmitted. If the value is	volatile memory, such as
	EPROMs, or other memory storage devices."); see also	set too high, then unnecessary delays will be	EEPROMs, FLASH EPROMs, or other memory
	col. 2:23-26; col. 4:38-41;	incurred before the start of	storage devices.")
	col. 28:1-17; col. 4:38-46;	transmission. The adapter	(004 2 01 07 (4)
	col. 2:21-27; col. 27:44- 28:17; see also Prosecution	generates an indication of an underrun condition which is	'094 patent at 2: 21-27 ("In one aspect of the invention,
	History: Specification as	made available to the host	the monitoring logic
	Filed, p. 52; Specification as	through the XMIT	includes a threshold store,
	Filed, p. 55; Specification as Filed, p. 58.	FAILURE register. If such	which is programmable by the host computer for
	1 116u, p. 30.	an underrun indication occurs, then the host driver	storing a threshold value

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2		evidence EXTRINSIC EVIDENCE:	should increase the value on	and logic for posting status
3		3Com's expert, Dr. Michael	the XMIT START	information to the host.
٦		Mitzenmacher may provide	THRESH register. Further	Thus, the threshold value
4		an expert report or other	underrun indications should	may be set by the host
		form of testimony regarding	cause the driver to	system to optimize
5		the technology to which this term relates and how a	continually increase the XMIT START THRESH	performance using the
		person having ordinary skill	value. If the XMIT START	alterable threshold store and the posted status
6		in the art in the field of	THRESH value is increased	information.")
7		networking technology	to a value of greater than the	,
′		would understand this term.	maximum length expected	'094 patent at 27:44-28:17
8		3Com reserves the right to	by the system, then the early	("XMIT START THRESH
9		rely on testimony by any expert in this action.	transmit start features should be disabled by	is used to specify the number of bytes of the
9		expert in this action.	writing a zero to the XMIT	transmit frame that must
10		See also U.S. Patent Nos.	START THRESH register."	reside on the adapter, ,
10		5,434,872; 5,732,094;	('094; Col. 28: 1-17).	before the adapter can
11		6,327,625; 6,526,446; and 6,570,884; Joint Claim	"ICh act massages 5	commence with the media access control functions
		Construction Statement in	"If host processor 5 responds to network adapter	associated with transmitting
12		Cv-05-00098 (VRW).	3 before a complete data	the frame
1.2			frame is transferred, host	The value for this register
13		3Com reserves the right to	processor 5 then may	may be programmed by the
14		rely on any statement made by any party under the	decrease the threshold value	host to optimize performance. If set too low,
17		Patent Local Rules.	in alterable storage location	system latencies or
15			10a enabling threshold logic 10 to generate the indication	bandwidth limitations may
			signal at a later time in the	cause the adapter to
16			next transfer of a data	underrun the network during transmission, causing a
17			frame. Alternatively, if host	partial frame with a
1 /			processor 5 responds to the	guaranteed bad CRC to be
18			network adapter 3 after a complete data frame has	transmitted. If the value is
			already been transferred,	set too high, then
19			host processor 5 may then	unnecessary delays will be incurred before the start of
			increase the threshold value	transmission")
20			in alterable storage location	
21			10a enabling the threshold logic to generate an	DICTIONARY/TREATISE
			indication signal at an	DEFINITIONS:
22			earlier time in the next	Webster's Ninth New
22			transfer of a data frame."	Collegiate Dictionary (Ninth
23			('459; Col. 6: 48-59).	Edition, 1988)
24			Diagram Dy/The ages	Alter: 1: to make different without changing into
- '			DICTIONARY/TREATISE DEFINITIONS:	something else
25			DEFINITIONS.	2: CASTRATE SPAY ~ vi:
			Webster's II New College	to become different syn see
26			<u>Dictionary</u> (2001), pg. 33:	CHANGE; alterable – adj.
27			Altering – "To make different."	The American Heritage
21			uniciciit.	Dictionary of the English
28		l	l	
			100	

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
			EXPERT TESTIMONY:	Language (4th Ed. 2000)
3			D-Link's expert, Howard	alter: v. tr. To change or make different; modify:
4			Frazier, may provide	altered my will. intr. To
5			testimony as to the definition of the disputed	change or become different.
3			terms as would be	<u>threshold</u>
6			understood by one of ordinary skill in the relevant	Webster's Ninth New
7			art and may provide an	Collegiate Dictionary
0			explanation of the technology.	(1983) Threshold - A level, point,
8				or value above which
9			D-Link also incorporates by reference Realtek's	something is true or will take place and below which
10			references.	it is not or will not.
				The American Heritage
11				Dictionary of the English Language (4th ed. 2000)
12				The point that must be
13				exceeded to begin producing a given effect or
				result or to elicit a response.
14				McGraw-Hill Electronics
15				Dictionary (fifth edition,
16				1994) Threshold: 1. The least
				value of a current, voltage,
17				or other quantity that produces the minimum
18				detectable response. It is also called a limen. 2. The
19				level of pumping at which a
				laser can go into self-excited oscillation.
20				
21				EXPERT TESTIMONY:
22				Realtek's expert, Dr. Izhak
				Rubin, may provide testimony as to the
23				definition of the disputed
24				terms as would be understood by one of
25				ordinary skill in the relevant
				art and may provide an explanation of the
26	"threshold value"	PRODUCED CONCEDUCTION:	PRODUCED CONCEDUCTION:	technology.  PROPOSED CONSTRUCTION:
27		PROPOSED CONSTRUCTION: A value representing the	PROPOSED CONSTRUCTION: A set value indicating a	A number corresponding to
28	found in claim	quantity of data sufficient to	desired limit.	a level of data required for
Z.01				

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
	(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
2	1	evidence	evidence	evidence
ا ا	numbers:	trigger the initiation of		some process to take place.
3	'094 patent: 47	transmission	Decemended.	DICTIONARY/TREATISE
4	094 patent. 47	DICTIONARY/TREATISE	REFERENCES:	DEFINITIONS:
4	also presented for	DEFINITIONS:	PATENT SPECIFICATION:	threshold
5	construction in:	See "threshold value" in	The following citations	
		subsection 1.	support D-Link's proposed	Webster's Ninth New
6	'459 patent: 1		claim construction.	Collegiate Dictionary
-		INTRINSIC EVIDENCE:		(1983)
7	'872 patent: 10	Claims: claim 7; claim 8;	"Coupled with the	Threshold - A level, point,
		claim 30; claim 31; claim 32; claim 45; claim 46;	threshold logic 36 is a	or value above which something is true or will
8		claim 47; claim 48; claim	threshold store 43 which	take place and below which
		49; claim 50; claim 51;	stores a <i>threshold value</i> which indicates an amount	it is not or will not.
9		claim 53; Specification: see,	of data of a frame that must	
10		<u>e.g.</u> , figs. 11-17col. 2:15-21	be resident in the frame	The American Heritage
10		("The network interface	buffer 34 before	Dictionary of the English
11		controller includes logic for initiating transmission of the	transmission of that frame	Language (4th ed. 2000) The point that must be
		frame when the threshold	may be initiated by the	exceeded to begin
12		determination indicates that	transmit DMA logic and	producing a given effect or
		a sufficient portion of the	MAC 39." ('094; Col. 4:	result or to elicit a response.
13		frame is resident in the	32-37) (emphasis added).	-
		transmit buffer, and prior to	"When the <i>threshold</i>	McGraw-Hill Electronics
14		the transfer of all of the data of the frame into the	amount of data is resident in	Dictionary (fifth edition,
15		transmit buffer"); see also	the buffer 34, then the	1994) Threshold: 1. The least
13		col. 2:20-26; col. 4:32-37;	transmit logic 39 is	value of a current, voltage,
16		col. 4:49-51; col. 18:10-12;	instructed to begin	or other quantity that
		col. 23:43-47; col. 23:56-67;	transmission of the frame.	produces the minimum
17		col. 24:1-3; col. 24:52-54;	The transmit logic 39 then begins retrieving data from	detectable response. It is
		col. 27:61-63; col. 4:59-5:3;	the buffer 34 to support	also called a limen. 2. The
18		col. 3:54-59; col. 20:10-36; 2:40-46; see also	transmission of the frame on	level of pumping at which a laser can go into self-excited
1.0		Prosecution History:	the medium 42. This	oscillation.
19		Specification as Filed, p. 52;	operation begins before the	020
20		Specification as Filed, p. 53;	entire frame has been transferred from the host	
20		Specification as Filed, p. 55;	computer 30 into the buffer	threshold value
21		Specification as Filed, p. 58;	34, if the transmit logic 39	McCarra IIII Flacturais
		Office Action, Mar. 19, 1996, p. 4.	is available to transmit the	McGraw-Hill Electronics Dictionary (fifth edition,
22		1770, p. 4.	frame subject of the ongoing	1994)
		EXTRINSIC EVIDENCE:	download from the host	Threshold Value: The
23		3Com's expert, Dr. Michael	computer 30, the frame	minimum input that
		Mitzenmacher may provide	being downloaded into the buffer 34 is larger than the	produces a corrective action
24		an expert report or other	threshold set by the	in an automatic control
25		form of testimony regarding the technology to which this	threshold store 43, and the	system.
23		term relates and how a	host computer 30 indicates	EXPERT TESTIMONY:
26		person having ordinary skill	that immediate transmission	
-		in the art in the field of	of the data is desired."	Realtek's expert, Dr. Izhak
27		networking technology	('094; Col. 4: 59-Col. 5: 3)	Rubin, may provide
		would understand this term.		testimony as to the
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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting
	evidence	evidence	evidence
	3Com reserves the right to	(emphasis added).	definition of the disputed
	rely on testimony by any	WEIG 1:11	terms as would be
	expert in this action.	"FIG. 1 illustrates a data	understood by one of
	See also U.S. Patent Nos.	communication system	ordinary skill in the relevant art and may provide an
	5,434,872; 5,732,094;	according to the present invention with a controller	explanation of the
	6,327,625; 6,526,446; and	circuit using a dedicated	technology.
	6,570,884; Joint Claim	transmit buffer memory	teemology.
	Construction Statement in	which is automatically	
	Cv-05-00098 (VRW).	enabled to begin	
		transmission of a frame on	
	3Com reserves the right to	the network when the	
	rely on any statement made	number of bytes available in	
	by any party under the	the transmit buffer memory	
	Patent Local Rules.	exceeds a preprogrammed	
		threshold." ('094; Col. 3:	
		54-59) (emphasis added).	
		(AD GEARE EUREGIA	
		"XMIT START THRESH	
		provides for an early start of transmission. The XMIT	
		START THRESH register is	
		used to specify the number	
		of transmit bytes that must	
		reside on the adapter before	
		it will start transmission.	
		Values greater than the	
		maximum frame length will	
		prevent this function from	
		operating properly. The	
		method for disabling this	
		function is to set the register	
		to zero. Bytes are counted	
		starting with the first byte of	
		the destination field of the	
		transmit frame. The number of bytes considered to be	
		available is the sum of the	
		immediate data written to	
		XMIT AREA by the host	
		and those bytes transferred	
		to the transmit data buffers	
		in the adapter using bus	
		master DMA operations.	
		The transmit request will be	
		posted immediately after	
		XMIT START THRESH	
		transmit frame bytes are	
		made available from the	
		immediate data or when the	
		adapter has bus-mastered	
		XMIT START THRESH-	
	1	XMIT IMMED LEN bytes	ĺ

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Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
(disputed terms in <b>bold</b> )	construction and supporting	construction and supporting	construction and supporting evidence
	evidence	onto the adapter. The	evidence
		number of bytes resident on	
		the adapter must be equal to	
		or greater than the value in	
		XMIT START THRESH	
		for the transmission to	
		commence, unless the total frame size is less than	
		XMIT START THRESH.	
		In that case, the frame will	
		begin transmission when the	
		entire frame has been copied	
		to the adapter. The actual	
		transmission of the frame may be delayed by previous	
		pending transmit frames and	
		by deferrals to network	
		traffic. This register is set	
		to zero during a reset."	
		('094; Col. 20: 10-36)	
		"The threshold logic	
		determines the amount of	
		immediate data from the	
		descriptor, and monitors the	
		downloading of data of the	
		frame into the download	
		area. When the combination meets the	
		threshold, then actual	
		transmission of the frame is	
		initiated. Thus,	
		transmission of a frame may	
		be initiated before the complete frame has been	
		downloaded into the	
		download area." ('094; Col.	
		2: 40-46) (emphasis added).	
		EXTRINSIC EVIDENCE:	
		EXTRINSIC EVIDENCE.	
		DICTIONARY/TREATISE	
		DEFINITIONS:	
		Webster's Ninth New	
		Collegiate Dictionary (1983), pg.229:	
		Threshold - "A level, point,	
		or value above which	
		something is true or will	
		take place and below which	
		it is not or will not."	

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1	Claim language	3Com's proposed	D-Link's proposed	Realtek's proposed
2	(disputed terms in <b>bold</b> )	construction and supporting evidence	construction and supporting evidence	construction and supporting evidence
3			EXPERT TESTIMONY:	
4			D-Link's expert, Howard Frazier, may provide	
5			testimony as to the definition of the disputed	
6			terms as would be understood by one of	
7			ordinary skill in the relevant art and may provide an	
8			explanation of the technology.	
9		<u> </u>	<u> </u>	<u> </u>

#### 4. <u>U.S. Pat. No. 6,327,625</u>

11			
	Claim language	3Com's proposed construction and	Realtek's proposed construction and
12	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
	"logic"	PROPOSED CONSTRUCTION: Circuitry and/or	Please refer to the construction under 35
13		programming	U.S.C. § 112 ¶ 6 for the separate claim
15	found in claim		limitations of the identified claims. To the
14	numbers:	DICTIONARY/TREATISE DEFINITIONS:	extent the term "logic" requires
17		See "logic" in subsection 1.	construction, Realtek asserts that "logic" (or
15	'625 patent: 23	_	"logic for") as used in the identified claims
13	-	INTRINSIC EVIDENCE:	should be construed as "means" (or "means
1.	also presented for	Claims: see, e.g., claim 2 ("2. The computer	for") and, therefore, the associated claim
16	construction in:	system of claim 1, comprising logic to	elements should be governed by 35 U.S.C.
		maintain a list of packets stored in the	§ 112 ¶ 6.
17	'459 patent: 1	buffer having the particular packet type, and	"
		wherein the logic to transfer packets is	EXPERT TESTIMONY:
18	'872 patent: 1, 21	responsive to the list."); claim 3 ("3. The	
	_	computer system of claim 1, comprising	Realtek's expert, Dr. Izhak Rubin and/or
19	'884 patent: 1	logic to set parameters associated with the	Dr. Nick Bambos, may provide testimony
		packets in the buffer having the particular	as to the definition of the disputed terms as
20		packets in the burlet having the particular packet type, and the logic to transfer	would be understood by one of ordinary
		packet type, and the logic to transfer packets is responsive to the parameters.");	skill in the relevant art and may provide an
21			explanation of the technology.
		claim 6 ("6. The computer system of claim	
22		1, wherein the logic to transfer the packets	
		includes processing resources which write a	
23		control field in the buffer in association	
		with each packet, indicating the type of	
24		packet, whether the packet is ready for	
		transfer, and whether the packet has already	
25		been transferred."; see also claim 1; claim	
		7; claim 8; claim 9; claim 10; claim 11;	
26		claim 12; claim 13; claim 23; claim 24;	
		claim 25; claim 28; claim 29; claim 30;	
27		claim 31; claim 33; claim 34; claim 35;	
41		Specification: see, e.g., figs. 1, 3-8; col. 2:9-	

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,			
1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
ار	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
4		14 ("Logic is included in the network	
2		interface to transfer packets out of the	
3		buffer to the other of the first and second	
4		ports according to the order of receipt, and	
4		according to the respective packet types so	
5		that packets having a particular packet type are transferred out of the order of receipt	
		relative to packets having other packet	
6		types."); col. 2:18-19 ("Logic maintains a	
		list of packets stored in the buffer having a	
7		particular packet type."); col. 2:44-3:12 ("In	
		yet another embodiment, the logic to	
8		transfer the packet includes processing	
		resources which perform, in various	
9		combinations and orders, the following	
		functions: set up a control field for each	
10		packet stored in the buffer in an order of	
		receipt; write a parameter in the control	
11		field indicating the packet type has one of a	
1.2		plurality of packet types, including a first	
12		packet type, a second packet type and a	
13		third packet type; write a parameter in the	
13		control field indicating whether the packet	
14		has already been transferred; maintain a queue of entries identifying packets having	
17		the third packet type; process packets	
15		having the second packet type according to	
		a particular process; write a parameter in	
16		the control field for packets having the	
		second packet type indicating whether the	
17		packet is ready for transfer and the	
		processing according to the particular	
18		process is complete; maintain an indicator	
		of fullness of the buffer; transfer a packet	
19		from the buffer according to a priority rule	
20		which causes transfer of a packet identified	
20		by an entry in the queue ahead of packets in	
21		the buffer having the first and second	
41		packet types relative to the order of receipt,	
22		causes transfer of a packet having the first packet type in the order of receipt of the	
		packet type in the order of receipt of the packet, if the parameters in the control field	
23		indicate the packet is ready for transfer, and	
		the queue of entries is empty or the	
24		indicator of fullness exceeds a threshold,	
		and skips transfer of a packet having the	
25		second packet type relative to the order of	
		receipt if the parameter in the control field	
26		indicates the processing is not complete.");	
		see also col. 2:19-21; col. 2:37-44; col.	
27		3:18-20; col. 3:29-33; col. 3:51-52; col.	

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1 Claim language	3Com's proposed construction and	Realtek's proposed construction and
(disputed terms in <b>b</b> o		supporting evidence
2	3:61-67; col. 4:26-35; col. 4:39-40; col.	
	5:25-27; col. 5:55-57; col. 5:60-64; col. 6:5-	
3	11; col. 6:31-32; col. 6:42-45; col. 7:10-15;	
	col. 8:1-6; col. 8:20-22; col. 8:28-30; col.	
4	8:51-52; col. 8:61-64; col. 9:47-50; col.	
	9:57-59; col. 9:65-67; col. 10:3-5; col. 10:5-	
5	6; see also Prosecution History: Response to	
	Office Action, May 1, 2001, p. 17-18;	
6		
<b>Ŭ</b>	Response to Office Action, May 1, 2001, p.	
7 <b>  </b>	18-19.	
7	Example of Example of	
	EXTRINSIC EVIDENCE:	
8	3Com's expert, Dr. Michael Mitzenmacher	
	may provide an expert report or other form	
9	of testimony regarding the technology to	
	which this term relates and how a person	
10	having ordinary skill in the art in the field	
	of networking technology would understand	
11	this term. 3Com reserves the right to rely on	
	testimony by any expert in this action.	
12		
	See also U.S. Patent Nos. 5,434,872;	
13	5,732,094; 6,327,625; 6,526,446; and	
	6,570,884; Joint Claim Construction	
14	Statement in Cv-05-00098 (VRW).	
17		
15	3Com reserves the right to rely on any	
13	statement made by any party under the	
1.6	Patent Local Rules.	
16 "logic to transfer	PROPOSED CONSTRUCTION: Circuitry and/or	PROPOSED CONSTRUCTION:
packets out of the	programming to transfer packets out of the	device that transfers packets out of the
buffer"	buffer.	buffer
10		
18 found in claim	DICTIONARY/TREATISE DEFINITIONS:	<u>DICTIONARY/TREATISE DEFINITIONS</u> :
numbers:	See "logic" in subsection 1 for definitions	
19	of that term, "frame transfer task" in	Synopsis, Inc., Electronic Design
'625 patent: 23	subsection 3 for definitions of "transfer,"	<u>Automation Glossary of Terms</u>
20	"packet types" in this section for	The sequence of functions performed by
	definitions of "packet" and "buffer" in	hardware or software. Hardware logic is
21	subsection 1.	made up of circuits that perform an
		operation. Software logic is the sequence of
22	INTRINSIC EVIDENCE:	instructions in a program.
	Claims: see, e.g., claim 28 ("the logic to	
23	transfer the packets includes processing	Newton's Telecom Dictionary:
ال دے	resources which write a control field in the	
24	buffer in association with each packet,	"Logica system that could be applied to
24	indicating the type of packet, whether the	the relationships between propositions to
25	packet is ready for transfer, and whether the	which only a binary choice of truth existed,
25	packet has already been transferred"); see	i.e., yes or no."
	also claim 1; claim 2; claim 3; claim 6;	
26	claim 7; claim 8; claim 9; claim 10; claim	IBM Dictionary of Computing (10th ed.
	11; claim 12; claim 13; claim 23; claim 24;	1993): The systematized interconnection of
27	claim 25; claim 29; claim 30; claim 31;	digital switching functions, circuits, or
	Ciann 25, Ciann 27, Ciann 50, Ciann 51,	devices.
28		
<b>-</b> ~	117	

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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
2		claim 33; claim 34; claim 35; Specification:	
_ ا		see, e.g., figs. 1, 3-8; col. 2:9-14 ("Logic is	EXPERT TESTIMONY:
3		included in the network interface to transfer	Dooltole's assessed Da I-bale Dubin man
,		packets out of the buffer to the other of the first and second ports according to the order	Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the
4		of receipt, and according to the respective	disputed terms as would be understood by
5		packet types so that packets having a	one of ordinary skill in the relevant art and
ااد		particular packet type are transferred out of	may provide an explanation of the
6		the order of receipt relative to packets	technology.
4		having other packet types"); see also col.	
7		2:19-21; col. 2:37-3:12; col. 3:29-33; col.	
´		3:61-67; col. 4:27-31; col. 8:4-9; col. 8:20-	
8		22; col. 8:28-30; col. 8:51-52; col. 8:61-64;	
		col. 9:47-50; col. 9:57-59; col. 9:65-67; col.	
9		10:3-5; see also Prosecution History: Response to Office Action, May 1, 2001, p.	
		17-18.	
10		17 10.	
_		EXTRINSIC EVIDENCE:	
11		3Com's expert, Dr. Michael Mitzenmacher	
ا ۱		may provide an expert report or other form	
12		of testimony regarding the technology to	
12		which this term relates and how a person	
13		having ordinary skill in the art in the field	
14		of networking technology would understand this term. 3Com reserves the right to rely on	
14		testimony by any expert in this action.	
15		testimony by any expert in this action.	
		See also U.S. Patent Nos. 5,434,872;	
16		5,732,094; 6,327,625; 6,526,446; and	
		6,570,884; Joint Claim Construction	
17		Statement in Cv-05-00098 (VRW).	
		1 11 1	
18		3Com reserves the right to rely on any	
		statement made by any party under the Patent Local Rules.	
19	"packet types"	PROPOSED CONSTRUCTION: Packets with	PROPOSED CONSTRUCTION: Packets with
_,∥	packet types	different formats and priorities	different formats or priorities.
20	found in claim	P. 101.00	F
21	numbers:	<b>DICTIONARY/TREATISE DEFINITIONS:</b> packet	DICTIONARY/TREATISE DEFINITIONS:
∠ 1    		type: Newton's Telecom Dictionary (17th	Webster's New World Dictionary (1991)
22	'625 patent: 23	ed. 2001): Packet type identifier: In packet	"type 4 a kind, class, or group having
		data networking technology, the third octet	distinguishing characteristics in
23		in the packet header that identifies the	common"
		packet's function and, if applicable, its sequence number.	
24		sequence number.	INTRINSIC EVIDENCE:
-		INTRINSIC EVIDENCE:	
25		Claims: see, e.g., claim 14 ("The computer	'625 patent, claim 26 ("The integrated
		system of claim 13, wherein the particular	circuit of claim 23, wherein the particular
26		type of packet comprises a priority packet,	type of packet comprises a priority
		and the second type of packet comprises a	packet.")
27		packet suitable for processing with a	
- 1			

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CI · I		
Claim language	3Com's proposed construction and	Realtek's proposed construction and
(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
	security protocol."); see also claim 1; claim	'625 patent, claim 27 ("The integrated
	2; claim 3; claim 7; claim 8; claim 9; claim	circuit of claim 23, wherein the particular
	10; claim 11; claim 12; claim 13; claim 15;	type of packet comprises a packet suitable
	claim 18; claim 19; claim 21; claim 22;	for processing with a security protocol.").
	claim 23; claim 24; claim 25; claim 26;	
	claim 27; claim 29; claim 30; claim 31;	'625 patent at 2:15-44 ("In one
	claim 33; claim 34; claim 35; Specification:	embodiment, a data filter is coupled with
	see, e.g., Figs. 2, 3 ("FIG. 3 is a diagram	the buffer to generate identifiers identifying
	illustrating the function of the packet filter	packets of data stored in the buffer as
	in the system of FIG. 1."); col. 2:44-3:12	members of one of a plurality of packet
	("In yet another embodiment, the logic to	types. Logic maintains a list of packets
	transfer the packet includes processing	stored in the buffer having a particular
	resources which perform, in various	packet type. The logic to transfer the
	combinations and orders, the following	packets is responsive to the list to determine
	functions: set up a control field for each	the order in which a given packet is
	packet stored in the buffer in an order of	transferred out of the buffer. <i>Thus for</i>
	receipt; write a parameter in the control	example, priority packets are identified an
	field indicating the packet type has one of a	entries placed in a queue of priority packe
		on the network interface In another
	plurality of packet types, including a first	embodiment, packets of the particular typ
	packet type, a second packet type and a	are suitable for processing according to a
	third packet type; write a parameter in the	process such as an encryption or
	control field indicating whether the packet	authentication process.")
	has already been transferred; maintain a	1
	queue of entries identifying packets having	
	the third packet type; process packets	'625 patent at 5:17-21 ("In this
	having the second packet type according to	embodiment, the packet filter identifies
	a particular process; write a parameter in	three classes of packets. The first type of
	the control field for packets having the	packet is <i>normal</i> packet is indicated by
	second packet type indicating whether the	branch 103. Second type of packet is the
	packet is ready for transfer and the	<i>IPsec</i> packet is the indicated by branch 10
	processing according to the particular	The third type of packet is the <i>priority</i>
	process is complete; maintain an indicator	packet as indicated by branch 105.")
	of fullness of the buffer; transfer a packet	
	from the buffer according to a priority rule	'625 patent, at 1:23-41 ("As computer
	which causes transfer of a packet identified	networks are adapted to carry a variety of
	by an entry in the queue ahead of packets in	types of traffic, network protocols are being
	the buffer having the first and second	developed to support variant processing of
	packet types relative to the order of receipt,	packets as they traverse the network. Thus
	causes transfer of a packet having the first	priority packets are developed which are
	packet type in the order of receipt of the	suitable for carrying real-time video or
	packet, if the parameters in the control field	audio signals Also, network security i
	indicate the packet is ready for transfer, and	supported for some types of packets. Thus
	the queue of entries is empty or the	the Internet security IPsec protocols are
	indicator of fullness exceeds a threshold,	being developed.")
	and skips transfer of a packet having the	(605
	second packet type relative to the order of	'625 patent, at 1:58-61 ("The present
	receipt if the parameter in the control field	invention provides support for priority and
	indicates the processing is not complete.");	Internet Protocol security packets, and
	see also col. 1:58-61; col. 2:5-9; col. 2:15-	other protocols at the network interface
	3:12; col. 4:11-13; col. 5:6-7; col. 5:17-21;	level and in conjunction with FIFO-based
	see also Prosecution History: Office Action,	packet buffers.") '625 patent, Abstract ("Support for priori

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4			
1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
2		Feb. 2, 2001, pp. 3-4; Response to Office	and IP security packets, and other protocols
		Action, May 1, 2001, p. 17-18; Response to	at the network interface level and in
3		Office Action, May 1, 2001, p. 18-19;	conjunction with FIFO-based packet buffers
		Response to Office Action, May 1, 2001, p.	is provided by allowing out of order
4		20.	processing of certain packets in the FIFO
-		20.	Logic is included in the network
5		EXTRINSIC EVIDENCE:	interface to transfer packets out of the
ا		3Com's expert, Dr. Michael Mitzenmacher	buffer according to the order of receipt, and
6		may provide an expert report or other form	according to the respective packet types so
		of testimony regarding the technology to	that packets having a particular packet type
7		which this term relates and how a person	are transferred out of the order of receipt
′		having ordinary skill in the art in the field	relative to packets having other packet
8		of networking technology would understand	types.")
0		this term. 3Com reserves the right to rely on	
9		testimony by any expert in this action.	<b>DICTIONARY/TREATISE DEFINITIONS:</b>
9		The state of the s	
1.0		See also U.S. Patent Nos. 5,434,872;	EXPERT TESTIMONY:
10		5,732,094; 6,327,625; 6,526,446; and	
1.1		6,570,884; Joint Claim Construction	Realtek's expert, Dr. Nick Bambos, may
11		Statement in Cv-05-00098 (VRW).	provide testimony as to the definition of the
			disputed terms as would be understood by
12		3Com reserves the right to rely on any	one of ordinary skill in the relevant art and
		statement made by any party under the	may provide an explanation of the
13		Patent Local Rules.	technology.
14			

#### 5. <u>U.S. Pat. No. 6,526,446</u>

4 -		<b>T</b>	Ţ
16	Claim language	3Com's proposed construction and	Realtek's proposed construction and
	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
17	"data download	PROPOSED CONSTRUCTION: A circuit that	PROPOSED CONSTRUCTION: The circuitry
	circuit"	retrieves data from memory	that downloads data corresponding to the
18			frame segment descriptor.
	found in claim	DICTIONARY/TREATISE DEFINITIONS:	
19	numbers:	See "data value" in subsection 6 for	Intrinsic Evidence:
		definitions of "data;" download: The	
20	'446 patent: 26	American Heritage Dictionary of the	'446 patent at 8:28-38 ("With reference still
_ "		English Language (4th ed. 2000): To	to FIG. 2, data download DMA circuit 212
21		transfer (data or programs) from a server or	utilizes the descriptors to retrieve and
- 1		host computer to one's own computer or	download the data file, TCP templates, IP
22		device; <u>circuit</u> : <u>The American Heritage</u>	templates, and frame header stored within
		<u>Dictionary of the English Language</u> (4th ed.	host memory 106 In other words, data
23		2000): The combination of a number of	download DMA circuit 212 receives the
23		electrical devices and conductors that, when	descriptor information from hardware
24		interconnected to a form a conducting path,	queue 210 and uses it to retrieve the actual
<b>24</b>		fulfill some desired function; see also	data stored within host memory 106.")
25		<u>Dictionary of Computing</u> (1st ed. 1983):	
23		Circuit: 1. The combination of a number of	'446 patent, Abstract ("Hardware only
26		electrical devices and conductors that, when	transmission control protocol segmentation
26		interconnected to form a conducting path,	for a high performance network interface
		fulfill some desired function. 2. A physical	card. Specifically, one embodiment of the
27		(electrical) connection used for	present invention includes a circuit for
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			,
1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
2	(disputed terms in <b>bold</b> )	supporting evidence communication. Dictionary of Computing	supporting evidence implementing transmission control protocol
		(3d ed. 1990): Circuit: The combination of a	(TCP) segmentation. The circuit includes a
3		number of electrical devices and conductors	segmentation circuit coupled to receive a
		that, when interconnected to form a	descriptor from a host device which
4		conducting path, fulfill some desired	corresponds to data. The segmentation
_		function.	circuit utilizes the descriptor to generate other descriptors that describe each frame
5		INTRINSIC EVIDENCE:	segment. Furthermore, the circuit also
6		Claims: see, e.g., claim 1 ("A circuit for	includes a data download circuit coupled to
		implementing transmission control protocol	the segmentation circuit to receive the
7		segmentation, said circuit comprising: a	frame segment descriptors. Specifically, the
		segmentation circuit coupled to receive a descriptor from a host device which	data download circuit retrieves the data from a memory. Moreover, the circuit
6 7 8 9		corresponds to data, said segmentation	includes a medium access control circuit
0		circuit utilizes said descriptor to generate a	coupled to the data download circuit to
9		frame segment descriptor; a data download	receive the data in a frame segment.")
10		circuit coupled to said segmentation circuit to receive said frame segment descriptor,	'446 patent, Fig. 2 (showing Host Driver
		said data download circuit retrieves said	202, Descriptor DMA 204, Segmentation
11		data from a memory; and a medium access	State Machine 208, Hardware Queue 210,
12		control circuit coupled to said data	Data Download DMA 212, etc.)
12		download circuit to receive said data in a frame segment."); claim 14 ("said data	'446 patent, Fig. 4 ("receiving from a host
13		download circuit comprises a data	device a descriptor signal corresponding to
		download direct memory access circuit");	data stored within memory; using the
14		see also claim 4; claim 8; claim 15; claim	descriptor signal to generate a frame
1.5		16; claim 18; claim 25; claim 26;	segment descriptor; receiving the data from
15		<u>Specification</u> : Fig. 2; Fig. 4; col. 2:29-34; col. 2:52-57; col. 2:54-67; 8:28-38.	the memory using a data download circuit, etc.)
16		001. 2.52 57, 001. 2.57 07, 0.20 50.	
		EXTRINSIC EVIDENCE:	DICTIONARY/TREATISE DEFINITIONS:
17		3Com's expert, Dr. Michael Mitzenmacher	circuit
1.0		may provide an expert report or other form of testimony regarding the technology to	Newton's Telecom Dictionary (eleventh ed.,
18		which this term relates and how a person	1996)
19		having ordinary skill in the art in the field	Circuit: The physical connection (or path) of
17		of networking technology would understand	channels, conductors and equipment
20		this term. 3Com reserves the right to rely on testimony by any expert in this action.	between two given points through which an electric current may be established. Includes
_		of any expert in this action.	both sending and receiving capabilities. A
21		See also U.S. Patent Nos. 5,434,872;	circuit can also be a network of circuit
22		5,732,094; 6,327,625; 6,526,446; and	elements, such as resistors, inductors,
		6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).	capacitors, semiconductors, etc., that performs a specific function. A circuit can
23		Statement in ev-03-00076 (VRW).	also be a closed path through which current
		3Com reserves the right to rely on any	can flow.
24		statement made by any party under the	
25		Patent Local Rules.	The American Heritage Dictionary of the English Language (4th ed. 2000)
23			The combination of a number of electrical
26			devices and conductors that, when
			interconnected to a form a conducting path,
27			fulfill some desired function.
28		<u> </u>	1
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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
2	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence download
_			download
3			The American Heritage Dictionary of the English Language (4th ed. 2000)
4			To transfer (data or programs) from a server or host computer to one's own computer or
5			device.  EXPERT TESTIMONY:
6			Realtek's expert, Dr. Nick Bambos, may
7			provide testimony as to the definition of the disputed terms as would be understood by
8			one of ordinary skill in the relevant art and
9			may provide an explanation of the technology.
10	"descriptor signal"	PROPOSED CONSTRUCTION: A signal that	PROPOSED CONSTRUCTION: A signal
10	found in claim	describes data.	indicating where the corresponding data is
11	numbers:	DICTIONARY/TREATISE DEFINITIONS:	in the host memory.
12	'446 patent: 26	See "descriptor" in this subsection and "indication signal" in subsection 1 for	INTRINSIC EVIDENCE:
	110 patent. 20	definitions of "signal."	'446 patent at 5:66-6:6 ("Referring to FIG.
13		INTRINSIC EVIDENCE:	2, <i>a host driver 202</i> running on processor 106 of host system 100 <i>is responsible for</i>
14		Claims: claim 26; claim 30; claim 31; claim	creating a descriptor for a data file stored
		32; claim 33; Specification: see, e.g., figs.	within host memory 106 which is to be
15		2-5; col. 2:43-46 ("the circuit includes a retriever circuit coupled to receive the first	eventually transferred by network interface card (NIC) 118 over network 120. <i>The</i>
16		signal from the host device which indicates	descriptor includes information about
1.7		where a descriptor is located within the host memory. The retriever circuit also retrieves	where the data file is stored within host memory 106, the size of the data file, along
17		the descriptor which describes data stored	with other information.")
18		within the host memory."); see also Fig. 4;	), AAC
1.0		col. 2:60-65; col. 3:23-26; col. 5:66-6:6; col. 6:19-22; col. 10:41-46; col. 11:1-4.	'446 patent at 6:19-22 ("More specifically, the descriptor structure prepared by host
19			driver 202 consists of control words,
20		EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher	fragment address, and fragment length. The control words contain packet related
21		may provide an expert report or other form of testimony regarding the technology to	information and flags.")
22		which this term relates and how a person	'446 patent, Abstract ("Hardware only
		having ordinary skill in the art in the field of networking technology would understand	transmission control protocol segmentation for a high performance network interface
23		this term. 3Com reserves the right to rely on	card The circuit includes a
24		testimony by any expert in this action.	segmentation circuit coupled to receive a descriptor from a host device which
		See also U.S. Patent Nos. 5,434,872;	corresponds to data. The segmentation
25		5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction	circuit utilizes the descriptor to generate other descriptors that describe each frame
26		Statement in Cv-05-00098 (VRW).	segment")
27		3Com reserves the right to rely on any	Fig. 4 (showing separate steps, including
		statement made by any party under the	"receiving from a host device a descriptor
28		121	

#### 1 Claim language Realtek's proposed construction and 3Com's proposed construction and (disputed terms in **bold**) supporting evidence supporting evidence Patent Local Rules. signal corresponding to data stored within memory") 3 DICTIONARY/TREATISE DEFINITIONS: Dictionary of Computing (3d ed. 1990): Stored information that describes how other information is stored, e.g. in an array, record, or file. By referring to the descriptor, a program can interpret the other The American Heritage Dictionary of the English Language (4th edition, 2000) A word, phrase, or alphanumeric character 9 used to identify an item in an information storage and retrieval system. 10 IBM Dictionary of Computing (10th ed. 11 A word or phrase used to categorize or 12 index information. 13 **EXPERT TESTIMONY:** 14 Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the 15 disputed terms as would be understood by one of ordinary skill in the relevant art and 16 may provide an explanation of the technology. 17 "a descriptor signal PROPOSED CONSTRUCTION: The descriptor 18 signal describes data stored within host which corresponds to data stored within memory. 19 memory" DICTIONARY/TREATISE DEFINITIONS: 20 found in claim See "descriptor" in this subsection for definitions of that term, "indication signal" numbers: 21 in subsection 1 for definitions of "signal," 446 patent: 26 "data value" in subsection 6 for definitions 22 of "data" and "buffer memory" in subsection 1 for definitions of "memory"; 23 correspond: The American Heritage Dictionary of the English Language (4th ed. 24 2000): To be in agreement, harmony, or conformity. To be similar or equivalent in 25 character, quantity, origin, structure, or function: English navel corresponds to Greek omphalos. See Synonyms at agree. 26 To communicate by letter, usually over a

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period of time.

27

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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
2		INTRINSIC EVIDENCE:	
		Claims: claim 1; claim 26; Specification:	
3		see, e.g., figs. 2-5; col. 2:43-46 ("the circuit	
		includes a retriever circuit coupled to	
		receive the first signal from the host device	
7		which indicates where a descriptor is	
_ ا		located within the host memory. The	
ااد		retriever circuit also retrieves the descriptor	
5 6		which describes data stored within the host	
6			
		memory."); see also col. 2:25-27; col. 2:60-	
7		62; col. 6:51-55; col. 10:40-42.	
		P	
8		EXTRINSIC EVIDENCE:	
		3Com's expert, Dr. Michael Mitzenmacher	
7 8 9		may provide an expert report or other form	
´		of testimony regarding the technology to	
10		which this term relates and how a person	
10		having ordinary skill in the art in the field	
_ <sub>1 1</sub>		of networking technology would understand	
11		this term. 3Com reserves the right to rely on	
12		testimony by any expert in this action.	
12			
		See also U.S. Patent Nos. 5,434,872;	
13		5,732,094; 6,327,625; 6,526,446; and	
		6,570,884; Joint Claim Construction	
14		Statement in Cv-05-00098 (VRW).	
15		3Com reserves the right to rely on any	
		statement made by any party under the	
16		Patent Local Rules.	
	"frame segment	PROPOSED CONSTRUCTION: A descriptor for	PROPOSED CONSTRUCTION: A descriptor
17	descriptor"	a frame segment.	identifying where the corresponding frame
-			segment is in the host memory.
18	found in claim	INTRINSIC EVIDENCE:	
10	numbers:	Claims: claim 1; claim 15; claim 26; claim	INTRINSIC EVIDENCE:
19		31; claim 32; claim 33; Specification: figs.	
17	'446 patent: 26	2-5; col. 2:29-31 ("the segmentation circuit	'446 patent at 6:58-7:14 ("Conversely, if
20	-	utilizes the descriptor to generate other	the data file needs TCP segmentation, TCP
20		descriptors that describe each frame	segmentation state machine 208 creates
		segment."); Fig. 4; col. 2:27-37; col. 2:50-	another set of descriptors wherein each
21		54; col. 2:63-65; col. 3:23-26; col. 6:58-	descriptor describes a fragment or a
		7:14; col. 10:44-57; col. 11:1-4.	segment of the data file. In other words, the
22			data file stored within host memory 106 is
		EXTRINSIC EVIDENCE:	virtually segmented down into a number of
23		3Com's expert, Dr. Michael Mitzenmacher	frames. Within the present embodiment,
		may provide an expert report or other form	each of the descriptors created by TCP
24		of testimony regarding the technology to	segmentation state machine 208 is going to
		which this term relates and how a person	contain a pointer to a location in host
25		having ordinary skill in the art in the field	memory 106 where a reusable "template"
		of networking technology would understand	for the IP header is stored. Furthermore,
26		this term. 3Com reserves the right to rely on	each descriptors is also going to contain a
20		testimony by any expert in this action.	pointer to a location in host memory 106
27		commony by any expert in this action.	where a reusable "template" for the TCP
41		See also U.S. Patent Nos. 5,434,872;	header is stored. Additionally, each of the
ຸ , ∥		<u>500 a150</u> 0.5. I atont 1105. 5,757,072,	neuder is stored. Adminorally, each of the
28			

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1	Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
2	(aispuiea ierms in <b>voia</b> )	5,732,094; 6,327,625; 6,526,446; and	descriptors would also include a control
-		6,570,884; Joint Claim Construction	word along with <i>pointers to where the data</i>
3		Statement in Cv-05-00098 (VRW).	file (payload) is stored within host memory
		20 1 114	106. Also, each descriptor contains a
4		3Com reserves the right to rely on any statement made by any party under the	pointer to a location in host memory 106 where a reusable template for the Medium
5		Patent Local Rules.	Access Control (MAC) header is stored.
			These descriptors are then transmitted by
6			TCP segmentation state machine 208 to
_			hardware queue 210 for temporary storage
/			As such, TCP segmentation state machine
8			208 transmits the revised structure
			descriptors to hardware queue 210 where
9			they are temporarily stored. <i>This revised</i> structure descriptor information stored
10			within hardware queue 210 will
10			subsequently be used by data download
11			DMA circuit 212 to transfer data.")
			'446 patent, Abstract ("Hardware only
12			transmission control protocol segmentation
13			for a high performance network interface
13			card. Specifically, one embodiment of the present invention includes a circuit for
14			implementing transmission control protocol
1.5			(TCP) segmentation. The circuit includes a
15			segmentation circuit coupled to receive a
16			descriptor from a host device which corresponds to data. <i>The segmentation</i>
			circuit utilizes the descriptor to generate
17			other descriptors that describe each frame
18			segment. Furthermore, the circuit also includes a data download circuit coupled to
			the segmentation circuit to receive the
19			frame segment descriptors. Specifically, the
20			data download circuit retrieves the data
20			from a memory. Moreover, the circuit includes a medium access control circuit
21			coupled to the data download circuit <i>to</i>
22			receive the data in a frame segment.
22			")
23			'446 patent, Fig. 4 ("receiving from a host
			device a descriptor signal corresponding to
24			data stored within memory; using the descriptor signal to generate a frame
25			segment descriptor; receiving the data from
			the memory using a data download circuit,
26			etc.)
27			'446 patent at 2: 27-37 ("The circuit
- '			includes a segmentation circuit coupled to
28			

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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
2			receive a descriptor from a host device
			which corresponds to data. The
3			segmentation circuit utilizes the descriptor
			to generate other descriptors that describe
4			each frame segment. Furthermore, the
_			circuit also includes a data download
5			circuit coupled to the segmentation circuit to receive the frame segment descriptors.
			Specifically, the data download circuit
6			retrieves the data from a memory.
7			Moreover, the circuit includes a medium
/			access control circuit coupled to the data
8			download circuit to receive the data in a
8			frame segment.")
9			
			EXPERT TESTIMONY:
10			Dooltole's ownert Dr. Niels Dombos, may
- 0			Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the
11			disputed terms as would be understood by
			one of ordinary skill in the relevant art and
12			may provide an explanation of the
			technology.
13			

#### 6. <u>U.S. Pat. No. 6,570,884</u>

3Com's proposed construction and

Claim language

Ciaini tanguage	Scom's proposed construction and	Reduced a proposed construction and
(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
"data value"	PROPOSED CONSTRUCTION: A value of	Realtek has asserted that claim 1 of the '884
	bit(s) of data.	patent is invalid under 35 U.S.C. § 112 ¶ 1
found in claim		or 2, because it is unclear what the claimed
numbers:	<u>DICTIONARY/TREATISE DEFINITIONS</u> :	"data value" is and the '884 patent
	data: Dictionary of Computing (1st ed.	specification fails to provide any written
'884 patent: 1	1983): Information that has been prepared,	description, support, or definition of the
_	often in a particular format, for a specific	term. In the event that the Court decides to
	purpose; see also Microsoft Computer	construe the term, Realtek asserts that it
	<u>Dictionary</u> (5th ed. 2002): Plural of the	should be construed as "one of a discard
	Latin datum, meaning an item of	command for discarding packets and a
	information; <u>Dictionary of Computing</u> (3d	continue command for letting packets
	ed. 1990): Information that has been	continue to the host."
	prepared, often in a particularly format, for	
	a specific purpose; Webster's New World	Intrinsic Evidence:
	Computer Dictionary (10th ed. 2003):	
	Factual information (such as text, numbers,	'884 patent at 10:30-35 ("When the ARM7
	sounds, and images) in a form that can be	is done processing the data, it can flush the
	processed by a computer. McGraw-Hill	packet from the FIFO by issuing either an
	Illustrated Telecom Dictionary (2d ed.	discard command or an continue command
	2000): In the communications industry,	via the Command register. The former
	data is anything that is transmitted or	command discards the packet while the latter
	processed digitally.	command lets the packet continue to the
		host.")
	<u>Intrinsic evidence</u> :	

Realtek's proposed construction and

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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
2		Claims: claim 1; claim 21; Specification:	'884 File History, Bates No. 3COM11743
		see, e.g., figs. 1, 3, 5; col. 10:31-35	(Rule 1.121 Marked-Up Claims), lines 11-13
3		("When the ARM7 is done processing the	("second logic coupled with the buffer, and
		data, it can flush the packet from the FIFO	responsive to the packet filter to read and
4		by issuing either an discard command or an	process data in the identified packets from
ا ۔		continue command via the Command register."); col. 10:49-53 ("the processor	the buffer, and to produce a data value dependent on contents of the packet prior to
5		may pull out data such as IP addresses or	transfer of the identified packets to the
		other data used at the interface, or the	second port but the first logic.")(underline
6		processor may initiate an action such as re-	text added to the claim during the
٦		boot or power up of the host processor, or	prosecution of the '884 patent.)
7		resetting the interface card"); see also col.	1 /
8		9:10-15; col. 9:24-26; col. 10:33-34; col.	DICTIONARY/TREATISE DEFINITIONS:
0		10:61-65; see also Prosecution History:	
9		RCE and Amendment, Aug. 15, 2002, p. 7;	data:
7		RCE and Amendment, Aug. 15, 2002, p.	
10		11; Response to Office Action, Jan. 22,	Dictionary of Computing (3d ed. 1990)
10		2003, p. 8; Notice of Allowance, Feb. 2,	Information that has been prepared, often in
11		2003, p. 2.	a particularly format, for a specific purpose
1 1		EXTRINSIC EVIDENCE:	Microsoft Computer Dictionary (5th ed.
12		3Com's expert, Dr. Michael Mitzenmacher	2002)
1-		may provide an expert report or other form	Plural of the Latin datum, meaning an item
13		of testimony regarding the technology to	of information
_		which this term relates and how a person	
14		having ordinary skill in the art in the field	Webster's New World Computer Dictionary
		of networking technology would	(10th ed. 2003): Factual information (such as
15		understand this term. 3Com reserves the	text, numbers, sounds, and images) in a form
		right to rely on testimony by any expert in	that can be processed by a computer.
16		this action.	EXPERT TESTIMONY:
		G 1 1/3 D 1 1/4 5 40 4 0 70	B 1/11
17		See also U.S. Patent Nos. 5,434,872;	Realtek's expert, Dr. Nick Bambos, may
		5,732,094; 6,327,625; 6,526,446; and	provide testimony as to the definition of the
18		6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).	disputed terms as would be understood by one of ordinary skill in the relevant art and
		Statement in CV-03-00078 (VKW).	may provide an explanation of the
19		3Com reserves the right to rely on any	technology.
•		statement made by any party under the	teemiology.
20		Patent Local Rules.	
	"first logic"	PROPOSED CONSTRUCTION: First Circuitry	Please refer to the construction under 35
21		and/or programming.	U.S.C. § 112 ¶ 6 identified below. To the
∥	found in claim		extent this term requires construction,
22	numbers:	DICTIONARY/TREATISE DEFINITIONS:	Realtek asserts that "logic" should be
22		See "logic" in subsection 1.	construed as "means" (or "means for") and,
23	'884 patent: 1		therefore, this claim element should be
24∥		INTRINSIC EVIDENCE:	governed by 35 U.S.C. § 112 ¶ 6. If the
24		See "logic" in this section.	Court determines that 35 U.S.C. § 112 ¶ 6
25		Extension Emperor:	does not apply, "first logic" should be
ا ا		EXTRINSIC EVIDENCE:  3Com's expert, Dr. Michael Mitzenmacher	construed as "first device."
26		may provide an expert report or other form	DICTIONARY/TREATISE DEFINITIONS:
20		of testimony regarding the technology to	DICTIONARI/TREATISE DEFINITIONS.
27		which this term relates and how a person	Synopsis, Inc., Electronic Design
۱ ا		having ordinary skill in the art in the field	Automation Glossary of Terms
28	<u> </u>	,	
-5		126	

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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
2	(disputed terms in <b>bold</b> )	supporting evidence of networking technology would	Supporting evidence  The sequence of functions performed by
_		understand this term. 3Com reserves the	hardware or software. Hardware logic is
3		right to rely on testimony by any expert in	made up of circuits that perform an
		this action.	operation. Software logic is the sequence of
4		See also U.S. Patent Nos. 5,434,872;	instructions in a program.
5		5,732,094; 6,327,625; 6,526,446; and	Newton's Telecom Dictionary:
		6,570,884; Joint Claim Construction	"Logica system that could be applied to
6		Statement in Cv-05-00098 (VRW).	the relationships between propositions to
7		3Com reserves the right to rely on any	which only a binary choice of truth existed,
/		statement made by any party under the	i.e., yes or no."
8		Patent Local Rules.	IBM Dictionary of Computing (10th ed.
			<u>1993</u> ): The systematized interconnection of
9			digital switching functions, circuits, or
10			devices.
			EXPERT TESTIMONY:
11			Realtek's expert, Dr. Nick Bambos, may
12			provide testimony as to the definition of the
			disputed terms as would be understood by
13			one of ordinary skill in the relevant art and may provide an explanation of the
1.4			technology.
14			es es
15	"host system"	PROPOSED CONSTRUCTION: A computer	PROPOSED CONSTRUCTION: Any system or
	found in claim	that communicates over a network.	computer that communicates over a network
16	numbers:	DICTIONARY/TREATISE DEFINITIONS:	Evidence
17	numbers.	Webster's New World Computer	
1 /		Dictionary (10th ed. 2003): 1. In the	(872: Col 1: lns. 65-67) (094: Col. 1, lns.
18	'884 patent: 1	Internet, any computer that can function as the beginning and end point of data	60-62) Furthermore, the prior art systems which use transmit data buffers require the
19		transfers. An Internet host has a unique	host or sending system to manage the
19		Internet address (called an IP address) and	transmit data buffer.
20		a unique domain name; <u>Dictionary of</u>	
		Computing (3d ed. 1990): Host computer	(872: Col. 3, ln. 65 to col. 4., ln. 2) (*094:
21		(host): A computer that is attached to a network and provides services other than	Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a
22		simply acting as a store-and-forward	host data processing system, generally
22		processor or communication switch.	referred to by reference number 1, which
23		The production of the producti	includes a host system bus 2, a host central
		INTRINSIC EVIDENCE: Claims: see, e.g., claim 1; claim 11; claim	processing unit 3, host memory 4, and other host devices 5, all communicating across the
24		12; claim 15; claim 16; claim 20; claim 21;	bus 2
25		claim 29; claim 30; claim 39; claim 40;	
23		claim 44; claim 45; Specification: see, e.g.,	(994 C 1 2 1 29 44) The control of th
26		col. 1:28-33 ("The NIC Device-Class Power Management Specification handles	(884: Col. 2, lns. 39-44) The invention is particularly suited to environments in which
27		the situation in which a host processor	the host system is actively handling
27		running Windows or another operating	communications and other processing tasks,

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Claim language	3Com's proposed construction and	Realtek's proposed construction and
(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
~ <b>  </b>	system OS wants to go to sleep, yet allow others to access any shared directories or	and in which the adapter is able to take over some specialized tasks without interfering
3	devices it might have offered to the	with the active processing in the host system.
	network."); col. 2:27-29 ("In another	with the delive processing in the nest system
4	embodiment the intercept technique of the	
	present invention is used for tracking the	
5 📗	host computer's IP address."); see also col.	
	1:8-11; col. 1:18-25; col. 1:33-38; col.	
5 <b>  </b>	1:66-2:5; col. 2:20-26; col. 2:29-45; col.	
_	3:19-22; col. 3:34-35; col. 4:11-13; col.	
7 📗	4:18-24; col. 4:46-51; col. 4:59-60; col.	
8	5:39-41; col. 7:2-5; col. 7:29-33; col. 9:6-	
? <b> </b>	15; col. 9:24-27; col. 10:33-34; col. 10:49-	
9	53; col. 1:16-17; col. 2:40-44; col. 4:37-	
ĺ∥	51;10:53-58; see also Prosecution History: Office Action, p. 5; Office Action, p. 6;	
0	Response to Office Action, May 14, 2001,	
	p. 6; Office Action, Jul. 26, 2001, p. 4;	
1∭	Office Action, Jul. 26, 2001, p. 6;	
	Response to Office Action, Oct. 26, 2001,	
2	p. 2; Final Office Action, Mar. 20, 2002, p.	
	4; Final Office Action, Mar. 20, 2002, p. 6;	
3	RCE and Amendment, Aug. 15, 2002, p. 7;	
.∭	RCE and Amendment, Aug. 15, 2002, p. 8;	
4	RCE and Amendment, Aug. 15, 2002, p.	
<u>.</u>	10; RCE and Amendment, Aug. 15, 2002,	
5	p. 11; RCE and Amendment, Aug. 15,	
6	2002, p. 12; Office Action, Nov. 4, 2002, p. 6; Office Action, Nov. 4, 2002, p. 8;	
	Response to Office Action, Jan. 22, 2003,	
7 📗	p. 8; Response to Office Action, Jan. 22,	
	2003, p. 9; Response to Office Action, Jan.	
3 <b>  </b>	22, 2003, p. 11; Response to Office Action,	
	Jan. 22, 2003, p. 13-14; Response to Office	
9	Action, Jan. 22, 2003, p. 15; Notice of	
<b>II</b> I	Allowance, Feb. 2, 2003, p. 2.	
0		
, <b>  </b>	EXTRINSIC EVIDENCE:	
1	3Com's expert, Dr. Michael	
2	Mitzenmacher, may provide an expert report or other form of testimony regarding	
<b>-</b>	the technology to which this term relates	
3	and how a person having ordinary skill in	
	the art in the field of networking	
4	technology would understand this term.	
	3Com reserves the right to rely on any	
5 📗	testimony given by any of the other experts	
	in this action.	
6		
<u>,  </u>	See also U.S. Patent Nos. 5,434,872;	
7 📗	5,732,094; 6,327,625; 6,526,446; and	
8	6,570,884; Joint Claim Construction	

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
(disputed terms in <b>bota</b> )	Statement in Cv-05-00098 (VRW).	supporting evidence
	3Com reserves the right to rely on any	
	position taken by the parties under the	
(2 • 22	Patent Local Rules.	
"logic"	PROPOSED CONSTRUCTION: Circuitry and/or programming	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 for the separate claim
found in claim numbers:	DICTIONARY/TREATISE DEFINITIONS: See "logic" in subsection 1.	limitations of separate claims. To the exter this term requires construction, Realtek asserts that "logic" (or "logic for") should be
'884 patent: 1	Intrinsic evidence:	construed as "means" (or "means for") and therefore, the associated claim elements
also presented for construction in:	Claims: see, e.g., claim 2 ("2. The interface of claim 1, wherein the second logic	should be governed by 35 U.S.C. § 112 ¶ 6 If the Court determines that 35 U.S.C. § 11
'459 patent: 1	comprises a general purpose processor module."); claim 7 ("7. The interface of	¶ 6 does not apply, "logic" should be construed as "device."
'872 patent: 1, 21	claim 2, wherein the first port, buffer, second port, packet filter, first logic and	DICTIONARY/TREATISE DEFINITIONS:
'625 patent: 23	processor comprise components of a single integrated circuit."); claim 11 ("11. The	Synopsis, Inc., Electronic Design Automation Glossary of Terms
	interface of claim 1, wherein the second logic to process the packet comprises a	The sequence of functions performed by hardware or software. Hardware logic is
	routine to discover an internet protocol IP address of the host system."); claim 12	made up of circuits that perform an operation. Software logic is the sequence o
	("12. The interface of claim 1, wherein the second logic to process the packet	instructions in a program.
	comprises a routine to issue a reboot command to the host system."); see also	Newton's Telecom Dictionary:  "Logica system that could be applied to
	claim 1; claim 8; claim 9; claim 10; claim 13; claim 14; claim 15; claim 16; claim 17;	the relationships between propositions to which only a binary choice of truth existed
	claim 18; claim 19; claim 20; claim 28; claim 31; claim 32; claim 33; claim 34;	i.e., yes or no."
	claim 37; claim 38; claim 39; claim 40; claim 41; claim 46; Specification: see, e.g., figs. 1-5; col. 1:61-66 ("The present"	IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of
	invention provides a network interface card, or an interface to other types of	digital switching functions, circuits, or devices.
	communication channels, with limited intelligence, implemented using a	EXPERT TESTIMONY:
	relatively slower, and lower cost embedded processor, supported by dedicated	Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the
	hardware logic for the purposes of intercepting certain packets being received	disputed terms as would be understood by one of ordinary skill in the relevant art and
	via the network."); col. 2:51-52 ("According to various aspects of the	may provide an explanation of the technology.
	invention, the packet filter comprises one or more match logic circuits."); see also	technology.
	col. 2:13-16; col. 2:52-53; col. 2:55-59; col. 2:65-3:10; col. 3:13-22; col. 3:35-39;	
	col. 3:41-43; col. 3:48-56; col. 3:65-67; col. 4:1-4; col. 4:16-17; col. 4:57-60; col.	
	4:63-65; col. 5:3-7; col. 5:37-38; col. 5:43-	

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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence
2		46; col. 5:50-6:7; col. 6:13-15; col. 6:21-	
3		24; col. 6:26-31; col. 6:33-35; col. 6:49-50;	
3		col. 6:62-63; col. 8:57-62; col. 10:3-5; col.	
4		10:61-65; see also Prosecution History: Office Action, p. 3; Office Action, p. 4;	
- '		Response to Office Action, May 14, 2001,	
5		p. 2; Response to Office Action, May 14,	
		2001, p. 3; Response to Office Action,	
6		May 14, 2001, p. 6; Office Action, Jul. 26,	
_		2001, p. 3; Office Action, Jul. 26, 2001, p.	
7		5; Response to Office Action, Oct. 26,	
8		2001, p. 2; Response to Office Action, Oct.	
°		26, 2001, p. 3; Final Office Action, Mar. 20, 2002, p. 3; Final Office Action, Mar.	
9		20, 2002, p. 5; Final Office Action, Mar. 20, 2002, p. 5; Final Office Action, Mar.	
<b>_</b>		20, 2002, p. 7; Final Office Action, Mar.	
10		20, 2002, p. 8; RCE and Amendment, Aug.	
		15, 2002, p. 7; RCE and Amendment, Aug.	
11		15, 2002, p. 8; RCE and Amendment, Aug.	
12		15, 2002, p. 10; RCE and Amendment,	
12		Aug. 15, 2002, p. 11; RCE and	
13		Amendment, Aug. 15, 2002, p. 12; Office Action, Nov. 4, 2002, pp. 4-5; Office	
		Action, Nov. 4, 2002, pp. 4-3, Office Action, Nov. 4, 2002, p. 7; Response to	
14		Office Action, Jan. 22, 2003, p. 8;	
		Response to Office Action, Jan. 22, 2003,	
15		p. 9; Response to Office Action, Jan. 22,	
1.0		2003, p. 11; Response to Office Action,	
16		Jan. 22, 2003, p. 12; Response to Office	
17		Action, Jan. 22, 2003, p. 13; Response to	
1 /		Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003,	
18		p. 15; Notice of Allowance, Feb. 2, 2003,	
		p. 2.	
19			
		EXTRINSIC EVIDENCE:	
20		3Com's expert, Dr. Michael Mitzenmacher	
21		may provide an expert report or other form of testimony regarding the technology to	
<u> </u>		which this term relates and how a person	
22		having ordinary skill in the art in the field	
		of networking technology would	
23		understand this term. 3Com reserves the	
_		right to rely on testimony by any expert in this action.	
24		tins action.	
25		See also U.S. Patent Nos. 5,434,872;	
25		5,732,094; 6,327,625; 6,526,446; and	
26		6,570,884; Joint Claim Construction	
20		Statement in Cv-05-00098 (VRW).	
27		3Com reserves the right to rely on any	
		Jeoni reserves the right to rery on any	

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Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and supporting evidence	Realtek's proposed construction and supporting evidence
(disputed terms in <b>both</b> )	statement made by any party under the	supporting evidence
	Patent Local Rules.	
	1 44040 2004 14400	
"read and process	PROPOSED CONSTRUCTION: read and	PROPOSED CONSTRUCTION:
data in the identified	process data in the identified packets from	read and process data in the identified
packets from the buffer"	the buffer	packets while the packets are in the buffer
C 1: 1:	INTRINSIC EVIDENCE:	INTRINSIC EVIDENCE:
found in claim	Claims: see, e.g., claim 37 ("logic which	2004 material of 6.26.27 (WTL
numbers:	signals the processor to process the data	'884 patent at 6:36-37 ("The processor
'884 patent: 1	after at least part of the identified packet is stored in the buffer"); claim 38 ("logic	accesses the packet from the receive FIFC 201 for processing.")
004 patent. 1	which signals the processor to process the	201 for processing.
	data after the identified packet is stored in	'884 File History, Bates No. 3COM11713.
	the buffer"); see also claim 1; claim 21;	lines 6-8 ("The present invention is directed
	claim 40; Specification: figs. 1-5; col.	to a network interface which has logic to
	6:38-40 ("In an alternative embodiment,	process packets in the frame buffer that are
	the packet is supplied in parallel to a RAM	identified by a packet filter as having a
	buffer which is independent of the receive	particular format, before the packets are
	FIFO"); Fig. 5; 6:36-37; 3:19-26; 6:58-7:7;	transferred to the host processor to which
	see also Prosecution History: RCE and	they are addressed.")
	Amendment, Aug. 15, 2002, p. 7; RCE and Amendment, Aug. 15, 2002, p. 11; RCE	'884 patent at 3:19-26 ("When a particular
	and Amendment, Aug. 15, 2002, p. 11, RCE and Amendment, Aug. 15, 2002, p. 12;	packet in the FIFO buffer reaches a stage
	Response to Office Action, Jan. 22, 2003,	upload to the host computer, the logic on t
	p. 8; Response to Office Action, Jan. 22,	network interface card issues an interrupt
	2003, p. 13-14; Notice of Allowance, Feb.	the processor on the network interface care
	2, 2003, p. 2.	if a flag is set. In response to the interrupt,
		the packet in the FIFO buffer is processed
	EXTRINSIC EVIDENCE:	locally on the network interface card. If the
	3Com's expert, Dr. Michael Mitzenmacher	FIFO buffer overflows during the processi
	may provide an expert report or other form	of the packet, then packets may be lost.")
	of testimony regarding the technology to	1004
	which this term relates and how a person	'884 patent at 6:58-7:7 ("FIG. 5 illustrates
	having ordinary skill in the art in the field	the processing which occurs upon
	of networking technology would understand this term. 3Com reserves the	interrupting the processor, and the handlin
	right to rely on testimony by any expert in	of the packet by the processor. The proces begins when a packet is at the top of the
	this action.	receive FIFO by testing the packet header
	tins action.	(block 400). The logic determines whether
	See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and	pattern match bit is set (block 41). If the pattern match bit is set, then the processor
	6,570,884; Joint Claim Construction	interrupted and the receive FIFO is stalled
	Statement in Cv-05-00098 (VRW).	(block 402) Upon receiving the
	Statement in ev 03 00000 (VRW).	interrupt, the processor handles the packet
	3Com reserves the right to rely on any	(block 403) Upon completion of
	statement made by any party under the	processing, the FIFO is "un-stalled" to be
	Patent Local Rules.	continued handling of the data flow (block
		405).")
		'884 File History, Bates No. 3COM11743
		(Rule 1.121 Marked-Up Claims), lines 11-
		("second logic coupled with the buffer, and
		( <u>second</u> togic coupled with the outler, and

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1	Claim language (disputed terms in <b>bold</b> )	3Com's proposed construction and	Realtek's proposed construction and
2	(aispaiea terms in <b>voia</b> )	supporting evidence	supporting evidence responsive to the packet filter to read and
			process data in the identified packets from
3			the buffer, and to produce a data value
			dependent on contents of the packet prior to transfer of the identified packets to the
7			second port but the first logic.") (underline
5			text added to the claim during the
			prosecution of the '884 patent.)
6			
7			'884 patent, Fig. 5 ("402 INTERRUPT
			PROCESSOR/STALL FIFO; <u>403</u> PROCESS PACKET; <u>404</u> DISCARD
8			PARKET [sic], MODIFY PACKET, OR DO
9			NOTHING TO PACKET; 404 "UN-
			STALL" FIFO"; 406 PROCEED)
10			EXPERT TESTIMONY:
11			Realtek's expert, Dr. Nick Bambos, may
12			provide testimony as to the definition of the
14			disputed terms as would be understood by one of ordinary skill in the relevant art and
13			may provide an explanation of the
1 4	<i>"</i>		technology.
14	"second logic"	PROPOSED CONSTRUCTION: Second Circuitry and/or programming	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 identified below. To the
15	found in claim	Circuity and of programming	extent this term requires construction,
	numbers:	DICTIONARY/TREATISE DEFINITIONS:	Realtek asserts that "logic" should be
16	'884 patent: 1	See "logic" in subsection 1.	construed as "means" and, therefore, this claim element should be governed by 35
17	004 patent. 1	INTRINSIC EVIDENCE:	U.S.C. § 112 ¶ 6. If the Court determines
1 /		See "logic" in this section.	that 35 U.S.C. § 112 ¶ 6 does not apply,
18		EXTRINSIC EVIDENCE:	"second logic" should be construed as "second device."
10		3Com's expert, Dr. Michael Mitzenmacher	second device.
19		may provide an expert report or other form	DICTIONARY/TREATISE DEFINITIONS:
20		of testimony regarding the technology to which this term relates and how a person	Synopsis, Inc., Electronic Design
ر ا		having ordinary skill in the art in the field	Automation Glossary of Terms
21		of networking technology would	The sequence of functions performed by
22		understand this term. 3Com reserves the right to rely on testimony by any expert in	hardware or software. Hardware logic is made up of circuits that perform an
		this action.	operation. Software logic is the sequence of
23		G 1 110 D 1 12 5 10 10 7	instructions in a program.
24		See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and	N. C. T.I. Divi
		6,570,884; Joint Claim Construction	Newton's Telecom Dictionary:
25		Statement in Cv-05-00098 (VRW).	"Logica system that could be applied to the relationships between propositions to
26		3Com reserves the right to rely on any	which only a binary choice of truth existed,
20		statement made by any party under the	i.e., yes or no."
27		Patent Local Rules.	IBM Dictionary of Computing (10th ed.
		<u>L</u>	

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1	Claim language	3Com's proposed construction and	Realtek's proposed construction and
2	(disputed terms in <b>bold</b> )	supporting evidence	supporting evidence 1993): The systematized interconnection of
3			digital switching functions, circuits, or devices.
4			EXPERT TESTIMONY:
5			Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the
6			disputed terms as would be understood by one of ordinary skill in the relevant art and
7			may provide an explanation of the technology.
8	"variant formats"	PROPOSED CONSTRUCTION: Varying	Proposed Construction:
9	found in claim	arrangements of packet information other than a destination MAC address	PROPOSED CONSTRUCTION: differing formats
10	numbers:	DICTIONARY/TREATISE DEFINITIONS:	DICTIONARY/TREATISE DEFINITIONS:
11	'884 patent: 1	variant: The American Heritage Dictionary of the English Language (4th ed. 2000):	<u>variant</u>
12		Having or exhibiting variation; differing.	The American Heritage Dictionary of the
13		INTRINSIC EVIDENCE: Claims: see, e.g., claim 9 ("the packet filter	English Language (4th Ed. 2000)
14		comprises: mask logic circuits, having a mask and a mask modifier logic to modify	adj. 1. Having or exhibiting variation; differing. 2. Tending or liable to vary;
15		the mask using the mask modifier in response to the packet; hash logic to	variable. 3. Deviating from a standard, usually by only a slight difference.
16		generate a hash in response to the packet and the mask; and compare logic to	EXPERT TESTIMONY:
17		compare the hash generated with an expected hash for one of the plurality of	Realtek's expert, Dr. Nick Bambos, may
18		variant formats."); see also claim 1; claim 8; claim 10; claim 16; claim 17; claim 18;	provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and
19		claim 19; claim 20; claim 21; claim 31; claim 32; claim 33; claim 34; claim 40;	may provide an explanation of the technology.
20		claim 41; claim 46; <u>Specification</u> : <u>see, e.g.</u> , figs. 4, 5; col. 2:52-53 ("The match logic circuits comprise mask logic circuits that	technology.
21		store a mask identifying selected bytes within a packet of a particular format in the	
22		plurality of variant formats."); see also col. 2:5-7; col. 3:16-19; col. 3:39-41; col. 3:48-	
23		52; col. 4:24-26; col. 5:3-5; <u>Prosecution</u> History: Response to Office Action, May	
24		14, 2001, p. 2; Response to Office Action, May 14, 2001, p. 3; Response to Office	
25		Action, May 14, 2001, p. 6; Office Action, Jul. 26, 2001, p. 3; Response to Office	
26		Action, Oct. 26, 2001, p. 2; Final Office Action, Mar. 20, 2002, p. 3; Final Office	
27		Action, Mar. 20, 2002, p. 7; Final Office Action, Mar. 20, 2002, p. 8; RCE and	
28		Amendment, Aug. 15, 2002, p. 10; RCE	
20			

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Claim language (disputed terms in bold)  and Amendment, Aug. 15, 2002, p. 11; RCE and Amendment, Aug. 15, 2002, p. 12; Office Action, Nov. 4, 2002, p. 5; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2.    EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.    See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).    3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	1	C1 · 1		D 1.11
and Amendment, Aug. 15, 2002, p. 11; RCE and Amendment, Aug. 15, 2002, p. 12; Office Action, Nov. 4, 2002, p. 5; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 13; Response to Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).  3Com reserves the right to rely on any statement made by any party under the	1		1 1	
RCE and Amendment, Aug. 15, 2002, p. 112, Office Action, Nov. 4, 2002, p. 5; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 13; Response to Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).	اء	(disputed terms in <b>bold</b> )		supporting evidence
12; Office Action, Nov. 4, 2002, p. 5; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 13; Response to Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2.  EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.  See also U.S. Patent Nos. 5, 434, 872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).  3Com reserves the right to rely on any statement made by any party under the	2			
Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 13; Response to Office Action, Jan. 22, 2003, p. 13; Response to Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2.    EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.    See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).    3Com reserves the right to rely on any statement made by any party under the				
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8 9 10 10 10 10 11 11 12 12 13 14 15 15 15 16 17 18 18 18 19 19 10 10 10 10 10 10 10 10 10 10 10 10 10			of Allowance, Feb. 2, 2003, p. 2.	
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3Com reserves the right to rely on any statement made by any party under the	14			
statement made by any party under the				
statement made by any party under the	15		3Com reserves the right to rely on any	
	10			
	16		1	
	10	,		

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# B. Claim Elements in Dispute as to Which Structures, Acts, or Materials the Elements Correspond Where the Parties Also Dispute Whether 35 U.S.C. § 112 ¶ 6 Applies

3				
4	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
4		structures, acts, or	structures, acts, or	structures, acts, or
5		materials to which the	materials to which the	materials to which the
6		elements correspond	elements correspond	elements correspond
	"means for comparing	3Com contends that 35	Fig. 14, comparator 213 and	Realtek contends that 35
7	the counter to the	U.S.C. § 112 ¶ 6 governs	RCV complete control 210.	U.S.C. § 112 ¶ 6 governs
8	threshold value in the	"means for comparing" (see Section C), but does not		both "means for comparing" and "means for
8	alterable storage	govern the additional		generating an indication
9		limitation of "generating."		signal" and identifies
1.0	location and generating	To the extent the Court		the corresponding
10	an indication signal to	finds § 112 ¶ 6 applicable to "generating," each of the		structures, acts, or materials as follows:
11	the host processor	above disclosures of "means		as follows.
	responsive to a	for comparing" are enabling		Figs. 12a-18 – receive
12	comparison of the	with respect to the generation of an indication		threshold logic
13	counter and the	signal to a host processor,		Figs. 19-23 – transfer
	alterable storage	e.g., "comparator 213"		threshold logic
14	location"	outputs data to "RCV		F: 24.20 1 1 1
15	location	COMPLETE control block 210" (see fig. 14, col.		Figs 24-28 – download transmit threshold logic
13		31, ln. 41), which generates		transmit threshold logic
16	found in claim	an indication signal (see col		Figs. 29-34 – transmit
1.7	numbers:	31, ln. 41-49); "EARLY		threshold logic
17		INDICATION LATCH block 512" (see col. 38, ln.		
18	'459 patent: 1	51-55); "early xmit		
	-	complete block" (see col.		
19		39, ln 57); and "AND gate		
20		616" (see fig. 31; col. 40, ln. 46); see also receive		
20		threshold logic (figs. 12a-		
21		18); transfer threshold logic		
		(figs. 19-23); download		
22		transmit threshold logic (figs. 24-28); transmit		
23		threshold logic (figs. 29-34).		
23	"transmit logic,	This is not a "means-plus-	Transmit MAC logic 39 in	Fig. 2 – transmit MAC
24	responsive to the	function" claim element	Fig. 2; network interface	Logic 39
25	means for initiating	subject to construction under	processor 14 in Fig. 3;	Fig. 3 – network interface
25	transmission, for	35 U.S.C. § 112 ¶ 6. The use of the word "means" in	elements 50, 66, and 67 in Fig. 4 and 4A; Xmit DMA	processor 14
26	·	claim drafting creates a	logic 109 in Fig. 5; transmit	
	retrieving data from	presumption that § 112 ¶ 6	DMA logic 155 in Fig. 9;	Fig. 4 – RAM interface 50,
27	the buffer memory	governs, while the absence of the word "means" in a	elements 320 and 321 in Fig. 12; elements 330, 331, and	transmit DMA 67, Ethernet transmitter 66
28	L	or the word incans in a	12, cicinemo 550, 551, and	transmitter 00
20				

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4	and supplying	particular claim element	332 in Fig. 13 elements 335,	
5	retrieved data for	creates a presumption that § 112 ¶ 6 is inapplicable. The	336, and 337 in Fig. 14; elements 340, 341, and 342	Fig. 4A – transmit DMA 67
3	transmission on the	subject of this element,	in Fig. 15; elements 350,	Fig. 5 – transmit DMA logic
6	communication	"transmit logic," is a well-	351, 353 [sic], 353, 354,	109, transceiver 105
7	medium"	known structure and its	355, 356, and 357 in Fig. 16,	Fig. 7 transmit descriptors
/		relationship to certain elements presumptively	and elements 400, 405, 407, 410, 411, and 413 in Fig. 18.	Fig. 7 – transmit descriptors
8	found in claim	governed by § 112 ¶ 6 is not	,,	Fig. 8 – transmit descriptor
		sufficient to bring it within		data structure
9	numbers:	the ambit of $\S 112 \P 6$ .		Fig. 9 – transmit descriptor
10		To the extent that the Court		ring buffer 152, transmit
	'872 patent: 1	finds this element to be		DMA logic 155
11		governed by 35 U.S.C. § 112 ¶ 6, such "transmit logic"		Fig. 12 – data available
12		disclosed in the specification		control block 323
		under 35 U.S.C. § 112 ¶ 6		
13		includes, without limitation:		Fig. 17 – state machine
14		"network adapter 6" (see fig. 1; col. 4, ln. 2-4, 16-17);		elements 370, 371, 372, 373
		"transmit logic 39" (see fig.		Fig. 18 – transmit data path
15		2; col. 4, ln. 38); " <b>network</b>		400, paths 401, 402, MUX
16		<b>adapter 6</b> " (see fig. 1; col. 4, ln. 2-4, 16-17); " <b>transmit</b>		410, transmit control logic 411
10		DMA module 67" (see figs.		711
17		4, 4A; col. 9, ln. 13-44); and		
18		"Ethernet transmitter module 66" (see fig.4; col.		
10		9, ln. 45-51); see also		
19		network interface processor		
20		14 (fig. 3); elements 50, 66, 67 (fig. 4 and 4A); Xmit		
20		DMA logic 109, transceiver		
21		105 (fig. 5); transmit		
22		descriptors (fig. 7); transmit descriptor data structure (fig.		
44		8); transmit descriptor ring		
23		buffer 152, transmit DMA		
24		logic 155 (fig. 9); elements 320 and 321 (fig. 12);		
<b>∠</b> +		elements 330, 331, and 332		
25		(fig. 13); elements 335, 336,		
26		and 337 (fig. 14); elements 340, 341, and 342 (fig. 15);		
∠0		elements 350, 351, 353 [sic],		
27		353, 354, 355, 356, and 357		
28		(fig. 16), and elements 400,		

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
-		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4		405, 407, 410, 411, and 413		
5		(fig. 18.) Fig. 12 – data available		
		control block 323		
6		E' 17 4 1'		
7		Fig. 17 – state machine elements 370, 371, 372, 373		
8		Fig. 18 – transmit data path		
		400, paths 401, 402, MUX		
9		410, transmit control logic		
10	"underrun control	This is not a "means-plus-	Underrun detector 413, and	Fig. 18 – CRC 404,
	logic, which detects a	function" claim element	elements 405, 407, 410, and	exclusive OR gate 407,
11	condition in which the	subject to construction under 35 U.S.C. § 112 ¶ 6. The use	411 in Fig. 18.	MUX 410, transmit control logic 411, underrun detector
12	means for transferring	of the word "means" in	"Communications Medium"	413
	falls behind the	claim drafting creates a		
13		presumption that § 112 ¶ 6 governs, while the absence	A network path through which frames are transmitted	
14	transmit logic, and	of the word "means" in a	or received.	
	supplies a bad frame	particular claim element		
15	signal to the	creates a presumption that §		
16	communications	112 ¶ 6 is inapplicable. The subject of this element,		
	medium in response to	"underrun control logic," is a		
17	the underrun	well-known structure and its		
18	condition"	relationship to certain elements presumptively		
		governed by § 112 ¶ 6 is not		
19	found in claim	sufficient to bring it within		
20	numbers:	the ambit of $\S 112 \P 6$ .		
	1141110015.	To the extent that the Court		
21	(072	finds this element to be		
22	'872 patent: 1	governed by 35 U.S.C. § 112 ¶ 6, such "underrun control		
		logic" disclosed in the		
23		specification under 35		
24		U.S.C. § 112 ¶ 6 includes, without limitation: "logic"		
_		(see col. 2, ln. 30); "host		
25		interface logic" (see fig. 2;		
26		col. 4, ln. 57); an "underrun detector" (see fig. 18, col.		
20		28, ln. 54); and " <b>XMIT</b>		
27		FAILURE register" (see		
28		col. 19, ln.14-38); see also		

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4		Underrun detector 413, and elements 404, 405, 407, 410, 411, 413 (fig. 18).		
5	"means, coupled with	While 3Com contends that	Early transmit logic 6A in	Fig. 2 – threshold logic 36,
6	the buffer memory	35 U.S.C. § 112 ¶ 6 governs	Fig. 1; threshold logic 36 in	threshold store 43
7	and including a host	"means for monitoring [the transferring of data]"	Fig. 2; network interface processor 14 in Fig. 3;	Fig. 3 – RAM 15
.	system alterable	(see Section C), the	download DMA 58 in Figs.	rig. 3 – KAIVI 13
8	threshold store for	limitation of "making a	4 and 4A; elements 300,	Fig. 5 – transmit descriptor
9		determination" is not governed by 35 U.S.C. § 112	301, 302, 303, 304, 305, 306, 307, 308, 309, 310,	and download DMA logic 107
9	storing a threshold	¶ 6. To the extent that the	311, 320, 321, 322, 323 in	107
10	value, for monitoring	Court determines that this	Figs. 11 and 12; elements	Fig. 11 – counter 300, AND
11	the transferring of data	limitation is governed by 35 U.S.C. § 112 ¶ 6, the	330, 331, and 332 in Fig. 13; elements 335, 336, and 337	Gate 301, delay circuit 302, adder 304, and D-type flip-
11	of a frame to the	limitation is disclosed in the	in Fig. 14; elements 340,	flops 305, 206
12	buffer memory to	specification, without	341, and 342 of Fig. 15;	F: 12
13	make a threshold	limitation, as: "threshold logic 36" (see fig. 2; col. 4,	elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig.	Fig. 12 – start threshold register 320, download
13	determination of an	ln. 30-31, 40-41, 67); see	16; and elements 370, 371,	compare clock 321, and
14	amount of data of the	also Early transmit logic 6A	372, and 373 in Fig. 17.	immediate data comparator
15	frame transferred to	(fig. 1); threshold store 43 (fig. 2); network interface		322
	the buffer memory"	processor 14, RAM 15 (fig.		Fig. 13 – threshold registers
16	-	3); download DMA 58 (figs.		330, 331, and threshold valid
17	found in claim	4 and 4A); transmit descriptor and download		register 332
	numbers:	DMA logic 107 (fig. 5);		Fig. 14 – threshold value
18	numoers.	elements 300, 301, 302, 303,		state diagram elements 335-
19	'872 patent: 10	304, 305, 306, 307, 308, 309, 310, 311, 320, 321,		37
	872 patent. 10	322, 323 (figs. 11 and 12);		Fig. 15 – comparator 340,
20		elements 330, 331, and 332		AND gate 341, comparator
21		in Fig. 13; elements 335, 336, and 337 (fig. 14);		342
		elements 340, 341, and 342		Fig. 16 – counter 350,
22		(fig. 15); elements 350, 351,		comparators 351-353, MUX
23		352, 353, 354, 355, 356, 357 (fig. 16); and elements 370,		354, and gate 355, comparator 357
		371, 372, and 373 (fig. 17).		, , , , , , , , , , , , , , , , , , ,
24		In addition redails the		
25		In addition, while the particular limitation of this		
		element that requires that		
26		these means be coupled to		
27		the buffer memory and include a host system		
		alterable threshold store are		
28			100	

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Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
	structures, acts, or	structures, acts, or	structures, acts, or
	materials to which the	materials to which the	materials to which the
	elements correspond	elements correspond	elements correspond
	not governed by 35 U.S.C. §		
	112 ¶ 6, such limitations are disclosed in connection with		
	such means as "threshold		
	<b>logic 36</b> " (see fig. 2; col. 4,		
	In. 30-31, 40-41), coupled to		
	a threshold store which "in a preferred system, is		
	dynamically programmable		
	by the host computer 30."		
((1)	(see fig. 2; col. 4, ln. 46-47).		
"data transfer	This is not a "means-plus- function" claim element	Host interface logic 31 in Fig. 2; network interface	Fig. 2 – host interface 31,
circuitry, having a	subject to construction under	processor 14 in Fig. 3 (and	bus 2
host system interface,	35 U.S.C. § 112 ¶ 6. The use	specifically elements 50, 51,	Fig. 3 – network interface
for transferring data	of the word "means" in	53, 55, and 58 in Figs. 4 and	processor 14, bus 13
of frames to the buffer	claim drafting creates a presumption that § 112 ¶ 6	4A); host interface logic 102, and Xmit descriptor and	Fig. 4 – RAM interface 50.
memory"	governs, while the absence	download DMA logic 107 in	host bus interface 51, EISA
memor y	of the word "means" in a	Fig. 5; and host descriptor	bus master interface 55,
2 1: 1:	particular claim element	logic 150 and download	master slave union 53,
found in claim	creates a presumption that §	DMA logic 151 in Fig. 9.	upload DMA 57, download DMA module 58
numbers:	112 ¶ 6 is inapplicable.		DIVIA IIIodule 36
	To the extent that the Court		Fig. 4A – download DMA
'872 patent: 21	finds this element to be		module 58, download DMA
	governed by 35 U.S.C. § 112 ¶ 6, such "data transfer		offset bus [12:2], download DMA byte enable [3.0]
	circuitry" is disclosed in the		DIVIA byte enable [5.0]
	specification and thereby		Fig. 5 – host interface logic
	enabled under 35 U.S.C. §		102, transmit descriptor
	112 ¶ 6 by: " <b>line 35</b> " (see fig. 2; col. 4, ln. 30); <u>see also</u>		logic, download DMA logi
	Host interface logic 31, bus		107
	2 (fig. 2); network interface		Fig. 9 – host descriptor log
	processor 14, bus 13 (fig. 3);		150, download DMA logic
	elements 50, 51, 53, 55, and 58, download DMA offset		151, transmit descriptor rin buffer 152
	bus [12:2], download DMA		burier 132
	byte enable [3.0] (figs. 4 and		Fig. 11 – adder 308, MUX
	4A); host interface logic		309, subtractor 310, registe
	102, and Xmit descriptor and		311
	download DMA logic 107 (fig. 5); and host descriptor		
	logic 150 and download		
	DMA logic 151, transmit		
	descriptor ring buffer 152		
	(fig. 9); adder 308, MUX		

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Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
	structures, acts, or	structures, acts, or	structures, acts, or
	materials to which the	materials to which the	materials to which the
	elements correspond	elements correspond	elements correspond
	309, subtractor 310, register 311 (fig. 11).		
"logic, coupled to the	This is not a "means-plus-	Early transmit logic 6A in	Figs. 11-12 – elements 300,
buffer memory, which	function" claim element subject to construction under	Fig. 1, threshold logic 36 in Fig. 2; network interface	302, 303, 304, 305, 306, 307, 308, 309 310, 311, 320
monitors the	35 U.S.C. § 112 ¶ 6. The use	processor 14 in Fig. 3;	321, 322, and 323
transferring of data of	of the word "means" in	download DMA 58 in Figs.	F: 16 1
a frame to the buffer	claim drafting creates a presumption that § 112 ¶ 6	4 and 4A; elements 300, 301, 302, 303, 304, 305,	Fig. 16 – elements 350, 351 352, 353, 354, 355, 356, an
memory to make a	governs, while the absence	306, 307, 308, 309, 310,	357
threshold	of the word "means" in a	311, 320, 321, 323 in Figs.	
determination of an	particular claim element creates a presumption that §	11 and 12; elements 330, 331, and 332 of Fig. 13;	
	112 ¶ 6 is inapplicable.	elements 335, 336, and 337	
amount of data of the	" 11	of Fig. 14; elements 340,	
frame transferred to	To the extent that the Court	341, and 342 of Fig. 15;	
the buffer memory"	finds this element to be governed by 35 U.S.C. § 112	elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig.	
	¶ 6, such "logic" disclosed in	16; and elements 370, 371,	
found in claim	the specification under 35	372, and 373 in Fig. 17.	
numbers:	U.S.C. § 112 ¶ 6 includes,		
1.4.1.0 \$1.0.	without limitation: "early transmit logic 6A" (see fig.		
	1; col. 4, ln. 11); "download		
'872 patent: 21	DMA logic 58" (see figs. 4,		
	4A; col. 23, ln. 22); "11 bit		
	<b>counter 300</b> " (see fig. 11; col. 23, ln. 30); and		
	"download		
	bytesResidentValue" (see		
	fig. 11; col. 24, ln. 9); see		
	also threshold logic 36 (fig. 2); network interface		
	processor 14 (fig. 3);		
	elements 301, 302, 303, 304,		
	305, 306, 307, 308, 309, 310, 311, 320, 321, 323		
	(figs. 11 and 12); elements		
	330, 331, and 332 (fig. 13);		
	elements 335, 336, and 337		
	(fig. 14); elements 340, 341, and 342 (fig. 15); elements		
	350, 351, 352, 353, 354,		
	355, 356, 357 (fig. 16); and		
	elements 370, 371, 372, and		
"logio posponsivo to	373 (fig. 17).	Trongmit MAC 1:- 20	Fig. 2. Almost -1.1.1i. 26
"logic, responsive to	This is not a "means-plus- function" claim element	Transmit MAC logic 39 in Fig. 2; network interface	Fig. 2 – threshold logic 36, threshold store 43

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4	the threshold	subject to construction under	processor 14 in Fig. 3;	
5	determination of the	35 U.S.C. § 112 ¶ 6. The use of the word "means" in	download DMA 58 in Figs. 4 and 4A; elements 320,	Fig. 3 – RAM 15
3	logic which monitors	claim drafting creates a	321, 322, and 323 in Fig. 12;	Fig. 5 – transmit descriptor
6	the transferring of	presumption that § 112 ¶ 6	elements 330, 331, and 332	and download DMA logic
7	data to the buffer	governs, while the absence of the word "means" in a	in Fig. 13; elements 335, 336, and 337 of Fig. 14;	107
´	memory, which	particular claim element	elements 340, 341, and 342	Fig. 11 – counter 300, AND
8	initiates transmission	creates a presumption that §	of Fig. 15; elements 370,	Gate 301, delay circuit 302,
9	of the frame from the	112 ¶ 6 is inapplicable.	371, 372, and 373 of Fig. 17, and elements 400, 405, 407,	adder 304 and D-type flip- flops 305, 306
	huffer memory to the	To the extent that the Court	410, 411, and 413 in Fig. 18.	
10	medium access	finds this element to be governed by 35 U.S.C. § 112	"Medium Access	Fig. 12 – start threshold register 320, download
11	controller prior to	¶ 6, such "logic" disclosed in	Controller"	compare block 321,
	_	the specification under 35		immediate data comparator
12	transfer of all of the	U.S.C. § 112 ¶ 6 includes, without limitation:	Circuitry or a device that controls access to the	322
13	data of the frame to	"transmit logic 39" (see fig.	network.	Fig. 13 – threshold registers
	the buffer memory,	2; col. 4, ln. 37-38); "start		330, 331, and threshold valid
14	including logic which	threshold register 320" (see fig. 12; col. 24, ln. 60-61);		register 332
15	initiates transmission	"download compare block		Fig. 14 – threshold valid
1.6	of the frame when no	<b>321</b> " (see fig. 12; col. 24, ln.		state diagram elements 335-337
16	complete frame of	61-62); "immediate data comparator 322" (see fig.		337
17	data is present in the	12; col. 24, ln. 64-65); and		Fig. 15 – comparator 340,
18	buffer memory"	"data available control block 323" (see fig. 12; col.		AND gate 341, comparator 342
10		24, ln. 67-68); see also		372
19	found in claim	threshold logic 36, threshold		Fig. 16 – counter 350,
20	numbers:	store 43 (fig. 2); network interface processor 14, RAM		comparators 351-353, MUX 354, and gate 355
		15 (fig. 3); download DMA		comparator 357
21	'872 patent: 21	58 (figs. 4 and 4A); transmit descriptor and download		
22		DMA logic 107 (fig. 5);		
		counter 300, AND Gate 301,		
23		delay circuit 302, adder 304 and D-type flip-flops 305,		
24		306 (fig. 11); elements 330,		
		331, and 332 (fig. 13);		
25		elements 335, 336, and 337 (fig. 14); elements 340, 341,		
26		and 342 (fig. 15); counter		
27		350, comparators 351-353, MUX 354, and gate 355		
27		comparator 357 (fig. 16);		
28				
- 11				

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1 Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2	structures, acts, or	structures, acts, or	structures, acts, or
	materials to which the	materials to which the	materials to which the
3	elements correspond	elements correspond	elements correspond
4	elements 370, 371, 372, and		
5	373 (fig. 17); and elements 400, 405, 407, 410, 411, and		
3	413 (fig. 18).		
6 "logic to transfer	This is not a "means-plus-		Fig. 1 – packet
packets out of the	function" claim element		upload/transmit control 24,
buffer to the other of	subject to construction under 35 U.S.C. § 112 ¶ 6.		out of order packet transfer control 25, priority queue 21
8 the first and second	The use of the word		control 23, priority queue 21
	"means" in claim drafting		Fig. 5 – elements 200, 201,
ports according to the	creates a presumption that §		202, 203, 204, 205, and 206
order of receipt, and	112 ¶ 6 governs, while the absence of the word		Fig. 6 – elements 150, 151,
according to the	"means" in a particular		152, 153, 154, 155, 156,
11 respective packet	claim element creates a		157, 158, 159, 160, 161,
types so that packets	presumption that § 112 ¶ 6		165, 167, 168, 169, 170,
having a particular	is inapplicable.		171, 172, and 173
packet type are	To the extent that the Court		Fig. 8 – ASIC 814, filters
	finds this element to be		and processing resources
transferred out of the	governed by 35 U.S.C. §		830, upload engine 825
order of receipt,	112 ¶ 6, such "logic" disclosed in the		
relative to packets	specification under 35		
16 having another packet			
17 type"	without limitation: "packet filter 14" (see fig. 1; col. 4,		
1 /	ln. 13); "FIFO(s) 13" (see		
18 found in claim	fig. 1; col. 4, ln. 2-5, 14);		
	"frame start header 16"		
19 numbers:	(see fig. 1; col. 4, ln. 15); "frame start header 17"		
20	(see fig. 1; col. 4, ln. 18);		
625 patent: 23	"top packet data 18" (see		
21	fig. 1; col. 4, ln. 18); " <b>IPsec</b>		
22	<b>queue 20</b> " (see fig. 1; col. 4, ln. 21); " <b>priority queue 21</b> "		
22	(see fig. 1; col. 4, ln. 21-22);		
23	"packet download/receive		
	control block 22" (see fig.		
24	1; col. 4, ln. 22-23); " <b>IPsec</b>		
25	packet processing resources 23" (see fig. 1;		
	col. 4, ln. 25); "packet		
26	upload/transmit control		
27	logic 24" (see fig. 1; col. 4,		
27	ln. 26); "out of order packet transfer control		
28	packet transfer control		
<sub> </sub>			

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4		<b>block 25</b> " (see fig. 1; col. 4,		
_		ln. 28); " <b>logic 26</b> " (see fig. 1; col. 4, ln. 29); " <b>logic 27</b> "		
5		(see fig. 1; col. 4, ln. 30);		
6		"memory arbitration logic		
7		28" (see fig. 1; col. 4, ln.		
/		34-35); " <b>multiplexer 29</b> " (see fig. 1; col. 4, ln. 35);		
8		"idle state 100" (see fig. 3;		
		col. 5, ln. 10); "state 101"		
9		(see fig. 3; col. 5, ln. 12);		
		"state 102" (see fig. 3; col.		
10		5, ln. 14); " <b>branch 103</b> " (see fig. 3; col. 5, ln. 20);		
11		"branch 104" (see fig. 3;		
11		col. 5, ln. 21); " <b>branch</b>		
12		<b>105</b> " (see fig. 3; col. 5, ln.		
1.0		22); "state 106" (see fig. 3;		
13		col. 5, ln. 24); " <b>state 107</b> "		
14		(see fig. 3; col. 5, ln. 29); "state 108" (see fig. 3; col.		
14		5, ln. 32); "state 120" (see		
15		fig. 4; col. 6, ln. 32); "state		
		<b>121</b> " (see fig. 4; col. 6, ln.		
16		38); "state 122" (see fig. 4; col. 6, ln. 46); "state 123"		
17		(see fig. 4; col. 6, ln. 49);		
1 /		"state 124" (see fig. 4; col.		
18		6, ln. 54); " <b>packet</b>		
1.0		transmit/upload logic 24"		
19		(see fig. 5; col. 7, ln 16); "idle state 200" (see fig. 5;		
20		col. 7, ln 17-18); "state		
20		<b>201</b> " (see fig. 5; col. 7, ln		
21		19); " <b>path 202</b> " (see fig. 5;		
		col. 7, ln 25); "align		
22		<b>pointer state 203</b> " (see fig. 5; col. 7, ln 25); " <b>branch</b>		
23		204" (see fig. 5; col. 7, ln		
23		25); " <b>state 205</b> " (see fig. 5;		
24		col. 7, ln 26); "data		
2.		transfer state 206" (see fig.		
25		5; col. 7, ln 29); " <b>branch 207</b> " (see fig. 5; col. 7, ln		
26		50); "retransmit state 208"		
-0		(see fig. 5; col. 7, ln 51);		
27		"branch 209" (see fig. 5;		
20		col. 7, ln 55); "flush state		
28				

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4		<b>210</b> " (see fig. 5; col. 7, ln		
ا ے		57); " <b>branch 211</b> " (see fig. 5; col. 7, ln 62); " <b>transfer</b>		
5		complete state 212" (see		
6		fig. 5; col. 7, ln 62-63); and		
		"resources 830" (see fig. 8;		
7		col. 13, ln. 48); <u>see also</u>		
8		elements 150, 151, 152, 153, 154, 155, 156, 157,		
		158, 159, 160, 161, 165,		
9		167, 168, 169, 170, 171,		
اا		172, and 173 (fig. 6); ASIC		
0		814, filters and processing resources 830, upload		
1		engine 825 (fig. 8).		
	"second logic coupled	This is not a "means-plus-		Fig. 1 – processor (slower)
2	with the buffer, and	function" claim element		14
3	responsive to the	subject to construction under 35 U.S.C. § 112 ¶ 6.		Fig. 2 – processor (slower
ااد	packet filter to read	The use of the word		than data path) 118,
4	-	"means" in claim drafting		including ARM 7 processor
	and process data in	creates a presumption that §		
5	the identified packets	112 ¶ 6 governs, while the absence of the word		Fig. 3 – processor 220
6	from the buffer, and	"means" in a particular		
	to produce a data	claim element creates a		
7	value dependent on	presumption that § 112 ¶ 6		
8	contents of the packet	is inapplicable.		
اار	prior to transfer of the	To the extent that the Court		
9	identified packets to	finds this element to be governed by 35 U.S.C. §		
0	the second port by the	112 ¶ 6, such "second logic"		
	1 0	disclosed in the		
1	first logic"	specification under 35		
2		U.S.C. § 112 ¶ 6 includes, without limitation:		
^∥	found in claim	"hardware filtering logic		
3	numbers:	<b>15</b> " (see fig. 1; col. 4, ln.		
		16); "embedded processor		
4	'884 patent: 1	<b>14</b> " (see fig. 1; col. 4, ln. 15-16); " <b>line 18</b> " (see fig. 1;		
5	1	col. 4, ln. 26); " <b>embedded</b>		
		processor 118" (see fig. 2;		
6		col. 5, ln. 8); "pattern		
7		match modules, modules 203, 204, 205 and 206" (see		
′′		fig. 3; col. 5, ln. 43);		
28				

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
-		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4		"packet classify unit 210"		
_		(see fig. 3; col. 5, ln. 44); "receive FIFO control		
5		logic 218" (see fig. 3; col. 6,		
6		ln. 29); "processor 220"		
		(see fig. 3; col. 6, ln. 36);		
7		"block 300" (see fig. 4; col.		
		6, ln. 45); "block 301" (see		
8		fig. 4; col. 6, ln. 47-48); "block 302" (see fig. 4; col.		
9		6, ln. 49); "block 303" (see		
		fig. 4; col. 6, ln. 50); "block		
10		<b>304</b> " (see fig. 4; col. 6, ln.		
		52); " <b>block 305</b> " (see fig. 4;		
11		col. 6, ln. 54); "block 306"		
		(see fig. 4; col. 6, ln. 55);		
12		"block 400" (see fig. 5; col. 6, ln. 61); "block 41" (see		
13		col. 6, ln. 63); "block 401"		
		(see fig. 5); "block 402"		
14		(see fig. 5; col. 6, ln. 64);		
		"block 403" (see fig. 5; col.		
15		7, ln. 2); "block 404" (see		
1.0		fig. 5; col. 7, ln. 5); "block		
16		<b>405</b> " (see fig. 5; col. 7, ln. 7); " <b>block 406</b> " (see fig. 5;		
17		col. 7, ln. 8); "ARM7		
1		<b>processor</b> " (col. 9, ln. 23);		
18		and "general purpose		
		processor module" (see		
19		col. 11, ln. 29).		

# C. Claim Elements that the Parties Agree Are Governed by 35 U.S.C. § 112 ¶ 6 but in Dispute as to Which Structures, Acts, or Materials the Elements Correspond

Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
	structures, acts, or	structures, acts, or	structures, acts, or
	materials to which the	materials to which the	materials to which the
	elements correspond	elements correspond	elements correspond
"means for comparing	"Means for comparing"		Fig. 2, includes without
the counter to the	disclosed in the specification under 35		limitation – threshold logic 10, alterable storage
threshold value in the	U.S.C. § 112 ¶ 6 includes,		location 10a, host processor
	without limitation: "logic		5, network adaptor 3

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4	alterable storage	<b>block 219</b> " (see fig. 14; col.		
_	location"	32, ln. 3); " <b>comparator 213</b> " (see fig. 14; col. 32, ln.		Figs. 12a-18, includes without limitation – register
5		25-26); "comparator 224"		221, counter 216, logic
6	found in claim	(see fig. 14; col. 32, ln. 46);		block 218, comparator 213,
7	numbers:	"comparator 318" (see fig. 21; col. 36, ln. 15);		register 223, comparator 224, logic block 222
/		"comparator 333" (fig. 23;		224, logic block 222
8	'459 patent: 1	col. 37, ln. 40);		Figs. 19-23, includes
9	ies parenti. I	"THRESHOLD COMPARE block 511"		without limitation. adder 317, comparator 318
9		(see fig. 24, 26; col. 38, ln.		317, comparator 316
10		42, 44); "comparator 517"		Figs. 24-28, includes
11		(see fig. 26; col. 38, ln. 2-5); "comparator 615" (see fig.		without limitation comparator 333
11		31; col. 40, ln. 41-45); see		Comparator 333
12		also threshold logic 10,		Figs. 29-34, includes
12		alterable storage location 10a, host processor 5,		without limitation, adder 614, comparator 615
13		network adaptor 3 (fig. 2);		014, comparator 013
14		register 221, counter 216,		
1.5		logic block 218, register		
15		223, comparator 224, logic block 222 (figs. 12a-18);		
16		comparator 318 (figs. 19-		
1.7	"	23); adder 614 (figs. 29-34).	II	Cas "masana havina a hast
17	"means for	The "means" disclosed in the specification under 35	Host interface logic 31 in Fig. 2; network interface	See "means, having a host system interface, for
18	transferring [data]"	U.S.C. § 112 ¶ 6 includes,	processor 14 in Fig. 3;	transferring data of frames
1.0		without limitation: "host	elements 50, 51, 53, 54, 55,	to the buffer memory."
19	found in claim	interface logic 31" (see fig. 2; col. 4, ln. 29; col. 5, ln.	and 58 in Figs. 4 and 4A; host interface logic 102 and	
20	numbers:	20); "download DMA	Xmit descriptor and	
21		<b>module 58</b> " (see fig. 4; col.	download DMA logic 107 in	
21	'872 patent: 1	8, ln. 55-col. 9, ln. 11); and "XMIT AREA register"	Fig. 5; and host descriptor logic 150 and download	
22		(see col. 18, ln. 6-10); <u>see</u>	DMA logic 151 in Fig. 9.	
22		also network interface		
23		processor 14 (fig. 3); elements 50, 51, 53, 54, and		
24		55 (figs. 4 and 4A); host		
		interface logic 102 and Xmit		
25		descriptor and download DMA logic 107 (fig. 5); and		
26		host descriptor logic 150 and		
		download DMA logic 151		
27		(fig. 9).		

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4	"means, having a host	The "means" disclosed in	Host interface logic 31 in	Fig. 1 – bus 2
5	system interface, for	the specification under 35 U.S.C. § 112 ¶ 6 includes,	Fig. 2; network interface processor 14 in Fig. 3;	Fig. 2 – host interface 31,
	transferring data of	without limitation: "host	elements 50, 51, 53, 54, 55,	bus 2
6	frames to the buffer	interface logic 31" (see fig. 2; col. 4, ln. 29; col. 5, ln.	and 58 in Figs. 4 and 4A; host interface logic 102 and	Fig. 3 – network interface
7	memory"	20); "download DMA	Xmit descriptor and	processor 14, bus 13
		<b>module 58</b> " (see fig. 4; col.	download DMA logic 107 in	E' A DAM' A C 50
8	found in claim	8, ln. 55-col. 9, ln. 11); and "XMIT AREA register"	Fig. 5; and host descriptor logic 150 and download	Fig. 4 – RAM interface 50, host bus interface 51, EISA
9	numbers:	(see col. 18, ln. 6-10); <u>see</u>	DMA logic 151 in Fig. 9.	bus master interface 55,
10		also bus 2 (fig. 1); host interface 31, bus 2 (fig. 2);		master slave union 53, download DMA module 57
	'872 patent: 1	network interface processor		
11		14, bus 13 (fig. 3); elements 50, 51, 53, 54, and 55, and		Fig. 4A – download DMA module 58, download DMA
12		download DMA offset bus		offset bus [12:2], download
12		[12:2], download DMA byte		DMA byte enable [3:0]
13		enable [3:0] (figs. 4 and 4A); host interface logic 102		Fig. 5 – host interface logic
14		and Xmit descriptor and		102, transmit descriptor and
15		download DMA logic 107 (fig. 5); and host descriptor		download DMA logic 107
		logic 150, download DMA		Fig. 9 – host descriptor logic
16		logic 151, and transmit descriptor ring buffer 152		150, download DMA logic 151, transmit descriptor ring
17		(fig. 9).		buffer 152
18	"means for	The "means" disclosed in the specification under 35	Early transmit logic 6A in Fig. 1; threshold logic 36 in	See "means, coupled with the buffer memory and
10	monitoring [the	U.S.C. § 112 ¶ 6 includes,	Fig. 2; network interface	including a host system
19	transferring of data]"	without limitation:	processor 14 in Fig. 3;	alterable threshold store for
20		"threshold logic 36" (see fig. 2; col. 4, ln. 30-31, 40-	download DMA 58 in Figs. 4 and 4A; elements 300,	storing a threshold value, for monitoring the transferring
	found in claim	41); "early transmit logic	301, 302, 303, 304, 305,	of data of a frame to the
21	numbers:	6A" (see fig. 1; col. 4, ln. 11); "download DMA logic	306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in	buffer memory to make a threshold determination of
22		<b>58</b> " (see figs. 4, 4A; col. 23,	Figs. 11 and 12; elements	an amount of data of the
23	'872 patent: 1	ln. 22); "11 bit counter 300" (see fig. 11; col. 23, ln.	330, 331, and 332 in Fig. 13; elements 335, 336, and 337	frame transferred to the buffer memory."
23		30); and " <b>download</b>	in Fig. 14; elements 340,	burier memory.
24		bytesResidentValue" (see	341, and 342 of Fig. 15;	
25		fig. 11; col. 24, ln. 9); see also network interface	elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig.	
		processor 14 (fig. 3);	16; and elements 370, 371,	
26		elements 301, 302, 303, 304, 305, 306, 307, 308, 309,	372, and 373 in Fig. 17.	
27		310, 311, 320, 321, 322, 323	"Monitoring"	
28		(figs. 11 and 12); elements		
20			1.47	

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4		330, 331, and 332 (fig. 13);	Watching, keeping track of,	
5		elements 335, 336, and 337 (fig. 14); elements 340, 341,	or checking on.	
5		and 342 (fig. 15); elements	Reference: 7, 12	
6		350, 351, 352, 353, 354,		
7		355, 356, 357 (fig. 16); and elements 370, 371, 372, and		
		373 (fig. 17).		
8	"means for	The "means" disclosed in the specification under 35	Transmit MAC logic 39 of Fig. 2; network interface	See "means, responsive to the threshold determination
9	initiating	U.S.C. § 112 ¶ 6 includes,	processor 14 in Fig. 3;	of the means for monitoring,
	[transmission]"	without limitation:	download DMA 58 in Figs.	for initiating transmission of
10		"transmit logic 39" (see fig. 2; col. 4, ln. 37-38);	4 and 4A; elements 320, 321, 322, and 323 in Fig.	the frame, prior to transfer of all the data of the frame
11	found in claim	"start threshold register	12; elements 330, 331, and	to the buffer memory from
1.0	numbers:	<b>320</b> " (see fig. 12; col. 24, ln. 60-61); "download	332 of Fig. 13; elements 335, 336, and 337 of Fig.	the host computer."
12		compare block 321" (see	14; elements 340, 341, and	
13	'872 patent: 1	fig. 12; col. 24, ln. 61-62); "immediate data	342 of Fig 15; elements 370, 371, 372, and 373 of Fig.	
1.4		comparator 322" (see fig.	17; and elements 400, 405,	
14		12; col. 24, ln. 64-65); and	407, 410, 411, and 413 in	
15		"data available control block 323" (see fig. 12; col.	Fig. 18.	
16		24, ln. 67-68); see also		
		network interface processor 14 (fig. 3); download DMA		
17		58 (figs. 4 and 4A);		
18		elements 330, 331, and 332 of Fig. 13; elements 335,		
19		336, and 337 of Fig. 14;		
19		elements 340, 341, and 342 (fig 15); elements 370, 371,		
20		372, and 373 (fig. 17); and		
21		elements 400, 405, 407, 410, 411, and 413 (fig. 18).		
21				
22	"means, responsive to	The "means" disclosed in the specification under 35	Transmit MAC logic 39 of Fig. 2; network interface	Fig. 1 – early transmit logic 6A
23	the threshold	U.S.C. § 112 ¶ 6 includes,	processor 14 in Fig. 3;	
	determination of the	without limitation:	download DMA 58 in Figs.	Fig. 2 – transmit MAC logic
24	means for monitoring,	"transmit logic 39" (see fig. 2; col. 4, ln. 37-38); "start	4 and 4A; elements 320, 321, 322, and 323 in Fig. 12;	Fig. 3 – network interface
25	for initiating	threshold register 320" (see	elements 330, 331, and 332	processor
26	transmission of the	fig. 12; col. 24, ln. 60-61); "download compare block	of Fig. 13; elements 335, 336, and 337 of Fig. 14;	Fig. 4 & 4A – transmit DMA
۷٥	frame prior to	<b>321</b> " (see fig. 12; col. 24, ln.	elements 340, 341, and 342	67
27	transfer of all the data	61-62); "immediate data comparator 322" (see fig.	of Fig 15; elements 370, 371, 372, and 373 of Fig. 17;	Fig. 5 – network interface
28		comparator 322 (See fig.	3/1, 3/2, and 3/3 of Fig. 1/;	rig. 3 – network interface
-5			1.40	

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4	of the frame to the	12; col. 24, ln. 64-65); and	and elements 400, 405, 407,	logic 104
5	buffer memory from	"data available control block 323" (see fig. 12; col.	410, 411, and 413 in Fig. 18.	Fig. 9 – transmit descriptor
	the host computer"	24, ln. 67-68); see also early	"Monitoring"	ring buffer 152, transmit
6		transmit logic 6A (fig. 1); transmit MAC logic (fig. 2);	Watahina kaonina trook of	DMA logic 155
7	found in claim	network interface processor	Watching, keeping track of, or checking on.	Fig. 12 – data available
	numbers:	14 (fig. 3); download DMA	D C 7 12	control block 323
8		58 and transmit DMA 67 (figs. 4 and 4A); network	Reference: 7, 12	Fig. 17 – state machine
9	'872 patent: 1	interface logic 104 (fig. 5);		elements 370, 371, 372, 373
10		transmit descriptor ring buffer 152, transmit DMA		Fig. 18 – transmit data path
10		logic 155 (fig. 9); elements		400, data paths 401-402,
11		330, 331, and 332 (fig. 13);		MUX 410 and transmit
12		elements 335, 336, and 337 (fig. 14); elements 340, 341,		control logic 411.
		and 342 (fig. 15); elements		
13		370, 371, 372, and 373 (fig. 17); and elements 400, 405,		
14		407, 410, 411, and 413 (fig.		
15	"[host interface]	The "means" disclosed in	Host interface logic 31 in	See "host interface means,
	means for	the specification under 35	Fig. 2; network interface	having an interface to the
16	transferring [data]"	U.S.C. § 112 ¶ 6 includes, without limitation: " <b>host</b>	processor 14 in Fig. 3 (and specifically elements 50, 51,	host system, for transferring data between the host system
17	81 1	interface logic 31" (see fig.	53, 54, 55, and 58 in Figs. 4	and the buffer memory."
18	found in claim	2; col. 4, ln. 29; col. 5, ln. 20); "download DMA	and 4A); host interface logic 102 (including Xmit	
10	numbers:	module 58" (see fig. 4; col.	descriptor and download	
19		8, ln. 55-col. 9, ln. 11); and	DMA logic 107 and View,	
20	'872 patent: 10	"XMIT AREA register" (see col. 18, ln. 6-10); see	Xfer, and Upload DMA logic 108) in Fig. 5; and host	
	_	also network interface	descriptor logic 150 and	
21		processor 14 (fig. 3); elements 50, 51, 53, 54, and	download DMA logic 151 in Fig. 9.	
22		55 (figs. 4 and 4A); host		
23		interface logic 102 (including Xmit descriptor		
		and download DMA logic		
24		107 and View, Xfer, and Upload DMA logic 108)		
25		(fig. 5); host descriptor logic		
26		150 and download DMA logic 151 (fig. 9).		
	"host interface means,	The "means" disclosed in	Host interface logic 31 in	Fig. 2 – host interface 31,
27	having an interface to	the specification under 35	Fig. 2; network interface	bus 2
28		U.S.C. § 112 ¶ 6 includes,	processor 14 in Fig. 3 (and	

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4	the host system, for	without limitation: "host	specifically elements 50, 51,	Fig. 3 – network interface
5	transferring data	interface logic 31" (see fig. 2; col. 4, ln. 29; col. 5, ln.	53, 55, 57, and 58 in Figs. 4 and 4A); host interface logic	processor 14, bus 13
	between the host	20); "download DMA	102 (including Xmit	Fig. 4 – RAM interface 50,
6	system and the buffer	module 58" (see fig. 4; col.	descriptor and download DMA logic 107 and View,	host bus interface 51, EISA bus master interface 55,
7	memory"	8, ln. 55-col. 9, ln. 11); and "XMIT AREA register"	Xfer, and Upload DMA	master slave union 53,
		(see col. 18, ln. 6-10); <u>see</u>	logic 108) in Fig. 5; host	upload DMA 57, download
8	found in claim	also host interface 31, bus 2 (fig. 2); network interface	descriptor logic 150 and download DMA logic 151 in	DMA module 58
9	numbers:	processor 14, bus 13 (fig. 3);	Fig. 9.	Fig. 4A – download DMA
1.0		elements 50, 51, 53, 55, and		module 58, download DMA
10	'872 patent: 10	57, download DMA offset bus [12:2], download DMA		offset bus [12:2], download DMA byte enable [3.0]
11		byte enable [3.0] (figs. 4 and		
12		4A); host interface logic 102 (including Xmit descriptor		Fig. 5 – host interface logic 102, transmit descriptor
12		and download DMA logic		logic and download DMA
13		107 and View, Xfer, and		logic 107
14		Upload DMA logic 108) (fig. 5); transmit area (fig.		Fig. 6 – transmit area
		6); transmit descriptors (fig.		
15		7); host descriptor logic 150, download DMA logic 151,		Fig. 7 – transmit descriptors
16		transmit descriptor ring		Fig. 9 – host descriptor logic
1.7		buffer 152 (fig. 9); adder		150, download DMA logic
17		308, MUX 309, subtractor 310, and register 311 (fig.		151, transmit descriptor ring buffer 152
18		11).		
19				Fig. 11 – adder 308, MUX 309, subtractor 310, and
19				register 311
20	"means, coupled with	The "means for monitoring"	Early transmit logic 6A in	Fig. 2 – threshold logic 36, threshold store 43
21	the buffer memory	disclosed in the specification under 35 U.S.C. § 112 ¶ 6	Fig. 1; threshold logic 36 in Fig. 2; network interface	threshold store 43
22	and including a host	includes, without limitation:	processor 14 in Fig. 3;	Fig. 3 – RAM 15
22	system alterable	"threshold logic 36" (see fig. 2; col. 4, ln. 30-31, 40-	download DMA 58 in Figs. 4 and 4A; elements 300,	Fig. 5 – transmit descriptor
23	threshold store for	41); "early transmit logic	301, 302, 303, 304, 305,	and download DMA logic
24	storing a threshold	6A" (see fig. 1; col. 4, ln. 11); "download DMA logic	306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in	107
	value, for monitoring	<b>58</b> " (see figs. 4, 4A; col. 23,	Figs. 11 and 12; elements	Fig. 11 – counter 300, AND
25	the transferring of	ln. 22); "11 bit counter	330, 331, and 332 in Fig. 13;	Gate 301, delay circuit 302,
26	data of a frame to the	<b>300</b> " (see fig. 11; col. 23, ln. 30); and " <b>download</b>	elements 335, 336, and 337 in Fig. 14; elements 340,	adder 304, and D-type flip- flops 305, 206
	buffer memory to	bytesResidentValue" (see	341, and 342 of Fig. 15;	
27	make a threshold	fig. 11; col. 24, ln. 9); see also threshold store 43 (fig.	elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig.	Fig. 12 – start threshold register 320, download
28		12.22	1,,,,,,	- O
			150	

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structures, acts, or materials to which the elements correspond elements correspond  determination of an amount of data of the frame transferred to the buffer memory"  found in claim  structures, acts, or materials to which the elements correspond elements correspond  2); network interface processor 14, RAM 15 (fig. 3); transmit descriptor and download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, and 12); elements 330, 331, regis  structures, acts, or materials to which the elements correspond elements 370, 371, immediately and 372, and 373 in Fig. 17.	nltek's proposed nctures, acts, or terials to which the ments correspond npare clock 321, and nediate data comparator  13 – threshold registers 331, and threshold valid lister 332
materials to which the elements correspond elements correspond elements correspond  determination of an amount of data of the frame transferred to the buffer memory"  found in claim numbers:  materials to which the elements correspond elements 370, 371, comprocessor 14, RAM 15 (fig. 3); transmit descriptor and download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, and 12); elements 330, 331, and 332 (fig. 13); elements  materials to which the elements correspond elements 370, 371, comprocessor 14, RAM 15 (fig. 3)72, and 373 in Fig. 17.	ments correspond  inpare clock 321, and inediate data comparator  13 – threshold registers in 331, and threshold valid
materials to which the elements correspond elements correspond elements of the frame transferred to the buffer memory"  found in claim numbers:  materials to which the elements correspond elements 370, 371, and 373 in Fig. 17.  materials to which the elements correspond elements 370, 371, and 372, and 373 in Fig. 17.  16; and elements 370, 371, 372, and 373 in Fig. 17.  16; and elements 370, 371, 372, and 373 in Fig. 17.  16; and elements 370, 371, 372, and 373 in Fig. 17.  17  18  19  10  10  11  12  13  13  14  15  16  17  17  18  18  19  19  19  19  19  19  19  19	npare clock 321, and nediate data comparator  13 – threshold registers 1, 331, and threshold valid
determination of an amount of data of the frame transferred to the buffer memory"         2); network interface processor 14, RAM 15 (fig. 3); transmit descriptor and download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, and 12); elements 330, 331, and 332 (fig. 13); elements         16; and elements 370, 371, immed 372, and 373 in Fig. 17.         comprise immed 322           6         the buffer memory"         (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, and 12); elements 330, 331, and 332 (fig. 13); elements         Fig. 372, and 373 in Fig. 17.         Fig. 360, 300, 300, 300, 300, 300, 300, 300,	npare clock 321, and nediate data comparator  13 – threshold registers 331, and threshold valid
amount of data of the frame transferred to the buffer memory"  found in claim numbers:  amount of data of the frame transferred to frame transferred to the buffer memory and download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, and 12); elements 330, 331, and 332 (fig. 13); elements  372, and 373 in Fig. 17.  372, and 373 in Fig. 17.	. 13 – threshold registers , 331, and threshold valid
5       amount of data of the frame transferred to the buffer memory"       3); transmit descriptor and download DMA logic 107       322         6       the buffer memory"       (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements       Fig. Fig. Fig. State	. 13 – threshold registers , 331, and threshold valid
frame transferred to the buffer memory" download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements	. 13 – threshold registers , 331, and threshold valid
the buffer memory"  (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements  (fig. 5); elements 300, 301, 330, regis  Fig. 320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements	, 331, and threshold valid
7   302, 303, 304, 305, 306, 307, 308, 309, 310, 311, regis   320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements   512, 512, 513, 513, 514, 514, 515, 514, 515, 515, 515, 515	
8 found in claim numbers:    320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements   Fig. state	ster 332
8 and 12); elements 330, 331, and 332 (fig. 13); elements	
and 332 (fig. 13); elements state	. 14 – threshold value
9	e diagram elements 335-
elements 340, 341, and 342 (fig. 15); elements 350, 351, Fig.	. 15 – comparator 340,
	D gate 341, comparator
11 (fig. 16); elements 370, 371, 342	
372, and 373 (fig. 17).	. 16 – counter 350,
	nparators 351-353, MUX
element are not governed by 354,	, and gate 355,
	nparator 357
subsection II.A.2 supra.  "means, responsive to The "means" disclosed in Transmit MAC logic 39 of Fig.	. 1 – early transmit logic
the threshold the specification under 35 Fig. 2; network interface 6A	t carry transmit logic
U.S.C. § 112 ¶ 6 includes, processor 14 in Fig. 3;	
" ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	. 9 – transmit descriptor g buffer 152, transmit
17	IA logic 155
for initiating threshold register 320" (see elements 330, 331, and 332	
	12 – data available
frame, prior to   "download compare block 321" (see fig. 12; col. 24, ln.   336, and 337 of Fig. 14; elements 340, 341, and 342   control	trol block 323
transfer of all the data 61-62); "immediate data of Fig 15; elements 370, Fig.	. 17 – state machine
20 of the frame to the comparator 322" (see fig. 17; and 373 of Fig. 17; elem 12; col. 24, ln. 64-65); and and elements 400, 405, 407,	ments 370, 371, 372, 373
	. 18 – transmit data path
the host computer"   block 323" (see fig. 12; col.   400,	, data paths 401-402,
22 22 24, ln. 67-68); see also early "Monitoring" MUX	X 410 and transmit
transmit logic 6A (fig. 1); network interface processor Watching, keeping track of,	trol logic 411.
14 in (fig. 3); download or checking on	
24 numbers: 1 DMA 58 (figs. 4 and 4A);	
transmit descriptor ring buffer 152, transmit DMA  keference: 7, 12	
'872 patent: logic 155 (fig. 9); data	
available control block 323	
(fig. 12); elements 330, 331,	
27 and 332 (fig. 13); elements 335, 336, and 337 (fig. 14);	

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Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
	structures, acts, or	structures, acts, or	structures, acts, or
	materials to which the	materials to which the	materials to which the
	elements correspond	elements correspond	elements correspond
	elements 340, 341, and 342		
	(fig 15); elements 370, 371, 372, and 373 (fig. 17);		
	elements 400, 401, 402, 405,		
	407, 410, 411, and 413 (fig.		
"[network interface]	18). The "network interface	Transmit MAC logic 39 of	See "network interface
	means" disclosed in the	Fig. 2; network interface	means, having an interface
means for	specification under 35	processor 14 in Fig. 3;	to the network transceiver
transferring [data]"	U.S.C. § 112 ¶ 6 includes,	elements 50, 66, and 67 in	and responsive to the means
	without limitation:	Fig. 4 and 4A; Xmit DMA	for initiating, for transferring
found in claim	"transmit logic 39" (see fig.	logic 155 in Fig. 9, elements	data between the buffer
	2; col. 4, ln. 38); "transmit	320 and 321 in Fig. 12;	memory and the network
numbers:	<b>DMA module 67</b> " (see figs. 4, 4A; col. 9, ln. 13-44);	elements 330, 331, and 332 in Fig. 13; elements 335,	transceiver for transmission."
	"Ethernet transmitter	336, and 337 in Fig. 14;	transmission.
'872 patent: 10	module 66" (see fig.4; col.	elements 340, 341, and 342	
-	9, ln. 45-51); "Ethernet	in Fig. 15; elements 350,	
	receiver module 62" (see	351, 353 [sic], 353, 354,	
	fig.4; col. 9, ln. 53-59);	355, 356, and 357 in Fig. 16,	
	"receive DMA module 63"	and elements 400, 405, 407,	
	(see figs. 4, 4A; col. 9, ln. 60-col. 10, ln. 12); and	410, 411, and 413 in Fig. 18.	
	"upload DMA module 57"	"Network"	
	(see figs. 4, 4A; col. 10, ln.	retwork	
	13-37); see also network	A system of computers,	
	interface processor 14 (fig.	terminals, and databases	
	3); elements 50 and 66 (figs.	connected by	
	4 and 4A); Xmit DMA logic	communications paths.	
	155 (fig. 9); elements 320 and 321 (fig. 12); elements	Reference: 7, 12	
	330, 331, and 332 (fig. 13);	Reference. 7, 12	
	elements 335, 336, and 337		
	(fig. 14); elements 340, 341,		
	and 342 (fig. 15); elements		
	350, 351, 352, 353, 354,		
	355, 356, and 357 (fig. 16);		
	and elements 400, 405, 407,		
"network interface	410, 411, and 413 (fig. 18). The "network interface	Transmit MAC logic 39 of	Fig. 3 – network interface
	means" disclosed in the	Fig. 2; network interface	processor 14,
means, having an	specification under 35	processor 14 in Fig. 3;	encoder/decoder 19
interface to the	U.S.C. § 112 ¶ 6 includes,	download DMA 58 in Figs.	Fig. 4 – cycle arbiter 56,
network transceiver	without limitation:	4 and 4A; elements 320,	interrupt controller 60,
and responsive to the	"network adapter 6" (see	321, 322, and 323 in Fig. 12;	Ethernet transmitter 66, and
_	fig. 1; col. 4, ln. 2-4, 16-17);	elements 330, 331, and 332	transmit DMA 67
means for initiating,	"transmit DMA module	of Fig. 13; elements 335,	Fig. 4A – transmit DMA 67
il .	<b>67</b> " (see figs. 4, 4A; col. 9,	336, and 337 of Fig. 14;	Fig. 5 – transmit DMA

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1	Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
2		structures, acts, or	structures, acts, or	structures, acts, or
		materials to which the	materials to which the	materials to which the
3		elements correspond	elements correspond	elements correspond
4	for transferring data	In. 13-44); "Ethernet	elements 340, 341, and 342	Logic 109
5	between the buffer	transmitter module 66" (see fig.4; col. 9, ln. 45-51);	of Fig. 15; elements 370, 371, 372, and 373 of Fig. 17;	Fig. 7 – transmit descriptors Fig. 9 – transmit descriptor
	memory and the	"Ethernet receiver module	and elements 400, 405, 407,	ring buffer 152, transmit
6	network transceiver	<b>62</b> " (see fig.4; col. 9, ln. 53-	410, 411, and 413 in Fig. 18.	DMA logic 155
7	for transmission"	59); "receive DMA module 63" (see figs. 4, 4A; col. 9,	"Network"	Fig. 18 – transmit data path 400, data paths 401-402,
		ln. 60-col. 10, ln. 12); and		MUX 410 and transmit
8	found in claim	"upload DMA module 57" (see figs. 4, 4A; col. 10, ln.	A system of computers, terminals, and databases	control logic 411
9	numbers:	13-37); see also Transmit	connected by	
		MAC logic 39 (fig. 2);	communications paths.	
10	'872 patent: 10	network interface processor 14 and encoder/decoder 19	Reference: 7, 12	
11	, , , , , , , , , , , , , , , , , , ,	(fig. 3); cycle arbiter 56,	1, 12	
12		download DMA 58, interrupt controller 60,		
12		Ethernet transmitter 66, and		
13		transmit DMA 67 (figs. 4		
14		and 4A); transmit DMA Logic 109 (fig. 5); transmit		
17		descriptors (fig. 7); transmit		
15		descriptor ring buffer 152,		
16		transmit DMA logic 155 (fig. 9); elements 320, 321,		
		322, and 323 (fig. 12);		
17		elements 330, 331, and 332 (fig. 13); elements 335, 336,		
18		and 337 (fig. 14); elements		
19		340, 341, and 342 (fig. 15);		
19		elements 370, 371, 372, and 373 (fig. 17); elements 400,		
20		401, 402 405, 407, 410, 411,		
21	"[control] means	and 413 (fig. 18). The "means for posting"	Info and Status registers in	See "control means, coupled
21	for posting [status	disclosed in the specification	Fig. 6; underrun detector 413	with the network interface
22	information]"	under 35 U.S.C. § 112 ¶ 6	in Fig. 18.	means, for posting status
23	mormation	includes, without limitation: "logic" (see col. 2, ln. 30);		information for use by the host system, as feedback for
	Carra d in adains	"host interface logic" (see		optimizing the threshold
24	found in claim	fig. 2; col. 4, ln. 57); an		value."
25	numbers:	"underrun detector" (see fig. 18, col. 28, ln. 54); and		
	(050	"XMIT FAILURE		
26	'872 patent: 10	register" (see col. 19, ln.14-38); see also Info and Status		
27		registers (fig. 6).		
		·	<u> </u>	

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Claim element	3Com's proposed	D-Link's proposed	Realtek's proposed
	structures, acts, or	structures, acts, or	structures, acts, or
	materials to which the	materials to which the	materials to which the
	elements correspond	elements correspond	elements correspond
"control means,	The "means for posting"	Info and Status registers in	Fig. 18 – transmit control
coupled with the	disclosed in the specification under 35 U.S.C. § 112 ¶ 6	Fig. 6; underrun detector 413 in Fig. 18.	logic 411 and underrun detector 413.
network interface	includes, without limitation:		
means, for posting	"logic" (see col. 2, ln. 30); "host interface logic" (see		
status information for	fig. 2; col. 4, ln. 57); an		
use by the host system,	"underrun detector" (see		
as feedback for	fig. 18, col. 28, ln. 54); and "XMIT FAILURE		
optimizing the	register" (see col. 19, ln.14-		
threshold value"	38); see also Info and Status registers (fig. 6); and transmit control logic 411		
found in claim	(fig. 18).		
numbers:			
'872 patent: 10			

# D. Claim Elements as to Which the Parties are in Dispute as to Whether 35 U.S.C. § 112 ¶ 6 Governs, but in Hypothetical Agreement as to Which Structures, Acts, or Materials the Elements Would Correspond

Claim element	Structures, acts, or	3Com's position as	D-Link's position as	Realtek's position as
	materials to which	to whether §112 ¶ 6	to whether §112 ¶ 6	to whether §112 $\P$ 6
	the elements	governs	governs	governs
	correspond			
"first logic coupled	To the extent that the	This is not a "means-	§112¶6 governs	§112¶6 governs
with the buffer and	Court finds this element to be	plus-function" claim element subject to		
the second port, to	governed by 35	construction under		
the second port, to transfer packets	U.S.C. § 112 ¶ 6, such "first logic"	35 U.S.C. § 112 ¶ 6. The use of the word		
from the buffer to	disclosed in the	"means" in claim		
the second port"	specification under 35 U.S.C. § 112 ¶ 6	drafting creates a presumption that §		
	includes, without	112 ¶ 6 governs,		
found in claim	limitation: "upload	while the absence of		
numbers:	engine 116" (see fig. 2) and "load engine	the word "means" in a particular claim		
	<u>I</u>	<u>l</u>	<u>l</u>	<u> </u>

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'884 patent: 1	<b>116</b> " (see col. 4, ln.	element creates a	
	64-65).	presumption that §	
		112 ¶ 6 is	
		inapplicable.	

In accordance with the Court's Standing Order 3.0, the parties attach copies of the 5, 307,459, 5,434,872, 5,732,094, 6,327,625, 6,526,446, and 6,570,884 patents as Exhibits D through I, respectively. The parties also make a complete prosecution history for each of these patents available to the Court upon request.

#### III. PATENT L.R. 4-3(c): TIME FOR CLAIM CONSTRUCTION HEARING

The parties believe that one day will be sufficient for the Claim Construction Hearing.

#### IV. PATENT L.R. 4-3(d): WITNESSES AT CLAIM CONSTRUCTION HEARING

Pursuant to Patent L.R. 4-3(d) and Standing Order 3.2, the parties understand that the court will not receive live testimony in connection with this claim construction hearing.

Attached are summaries of opinions to be offered by 3Com Corporation's expert, by Realtek Semiconductor Corp.'s experts Drs. Izhak Rubin and Nick Bambos, and a statement from D-Link Systems Inc.'s expert Mr. Howard Frazier, at Exhibits A-C respectively.

# V. PATENT L.R. 4-3(e): OTHER ISSUES FOR PRE-CLAIM CONSTRUCTION HEARING CONFERENCE

The parties have not identified any other issues which might appropriately be taken up at a prehearing conference prior to the Claim Construction Hearing.

Dated: January 18, 2006 Respectfully Submitted,

SIMPSON THACHER & BARTLETT LLP
By: \s\Henry B. Gutman
Henry B. Gutman (admitted *pro hac vice*)

	Case3:03-cv-02177-VRW Doo	eument303 Filed01/18/06 Page156 of 195		
1 2		Attorneys for Plaintiff/Counterdefendant 3Com Corporation		
3	Dated: January 18, 2006	Respectfully Submitted,		
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8	Dated: January 18, 2006	Respectfully Submitted,		
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12		Attorneys for Defendant/Counterplaintiff		
13		D-Link Systems, Inc.		
14				
15	Pursuant to General Order No. 45, Section X(B) regarding signatures, I attest under			
16		in the filing of this document has been obtained from Elizabeth		
17	H. Rader and Steven H. Morrissett.  Dated: January 18, 2006			
18	Dated: January 10, 2000	SIMPSON THACHER & BARTLETT LLP By: \s\ Henry B. Gutman		
19 20		Henry B. Gutman (admitted <i>pro hac vice</i> )		
21		Attorneys for Plaintiff/Counterdefendant		
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#### **EXHIBIT A**

#### STATEMENT OF 3COM CORP.'S EXPERT, DR. MICHAEL MITZENMACHER

#### A. QUALIFICATIONS

Dr. Michael Mitzenmacher graduated *summa cum laude* with a degree in mathematics and computer science from Harvard in 1991. After studying math for a year in Cambridge, England, on the Churchill Scholarship, Dr. Mitzenmacher obtained his Ph.D. in computer science at University of California at Berkley in 1996. Dr. Mitzenmacher then worked at Digital Systems Research Center until joining the Harvard faculty in 1999.

Dr. Mitzenmacher is a Professor of Computer Science in the Division of
Engineering and Applied Sciences at Harvard University. Dr. Mitzenmacher has authored or coauthored over 100 conference and journal publications on a variety of topics, including Internet
algorithms, hashing, load-balancing, erasure codes, error-correcting codes, compression, binpacking, and power laws. Dr. Mitzenmacher's work on low-density parity-check codes shared the
2002 IEEE Information Theory Society Best Paper Award. Dr. Mitzenmacher's first textbook on
probabilistic techniques in computer science, co-written with Eli Upfal, was published in 2005 by
Cambridge University Press.

#### B. TESTIMONY

#### 1. <u>Level of Ordinary Skill in the Art</u>

3Com may provide an expert report from Dr. Mitzenmacher regarding the general purpose and use of network interface cards and Ethernet networking technology, as well as the specific network interface cards of the patents-in-suit. Dr. Mitzenmacher's report may also provide information as to the level of experience, knowledge, and skill typical of a person having ordinary skill in those arts concerned with the technology disclosed in the patents-in-suit and how the terms proposed collectively by both sides in this action for construction are used by a person

having ordinary skill in the art, and specifically how such a person would interpret such terms in the context of the respective specifications, claims and prosecution histories of the patents-in-suit.

Such an expert report may further provide information as to the structure(s), act(s), and/or material(s), and equivalents thereof, disclosed in the respective specifications of the patents-in-suit or known to a person having ordinary skill in the art for each claim element found by the court to be governed by 35 U.S.C. § 112(6).

#### 2. The Meaning of Claims Terms

The following section details Dr. Mitzenmacher's opinions regarding how one of ordinary skill in the art in the field of networking technology would understand the disputed claim terms:

#### a. "alterable storage location"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent No. 5,307,459, should be construed to mean "storage location whose value is changeable."

#### b. "buffer"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, 5,732,094, 6,327,625, and 6,570,884, should be construed to mean "A memory for temporary storage of data."

#### c. "buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, and 5,732,094, should be construed to mean "A memory for temporary storage of data."

#### d. "indication signal"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,307,459, should be construed to mean "a signal that indicates a subsequent action, such as an interrupt."

#### e. "logic"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, 6,327,625, and 6,570,884, should be construed to mean "circuitry and/or programming."

#### f. "threshold value"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, and 5,732,094, should be construed to mean "a value representing the quantity of data sufficient to trigger the initiation of transmission."

#### g. "falls behind"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872,

should be construed to mean "underruns."

# h. "a condition in which the means for transferring falls behind the transmit logic"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872, should be construed to mean "a transmission underrun condition."

#### i. "underrun"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "When expected data from a frame to be transferred is not available."

### j. "underrun control logic"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872, should be construed to mean "logic that detects underruns."

#### k. "bad frame signal"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "a signal that a frame is bad."

#### l. "feedback"

In light of his review of the patent, prosecution history, and specification, in

connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "information from output returned to the input."

#### m. "optimizing the threshold"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "attempting to make the transmission of frames more efficient."

# n. "logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872, should be construed to mean "threshold logic that begins transmission of a frame before all data in the frame is within the buffer memory."

#### o. "threshold amount of data"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,732,094, should be construed to mean "an amount representing the quantity of data of a frame sufficient to trigger the initiation of transmission."

#### p. "altering the threshold"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, Dr. Mitzenmacher will assert that the underlined term, as it appears in U.S. Patent No. 5,732,094, should be construed to mean "changing."

#### q. "logic to transfer packets out of the buffer"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "circuitry and/or programming to transfer packets out of the buffer."

#### r. "order of receipt"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "order of receipt."

#### s. "packet types"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "packets with different formats and priorities."

t. "transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "data frames are transferred to the other of the host and the network

from the buffer within each packet type according to the order of receipt."

#### u. "data download circuit"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "a circuit that retrieves data."

#### v. "descriptor signal"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "a signal that describes data."

## w. "a descriptor signal which corresponds to data stored within memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "the descriptor signal describes the data stored within host memory."

#### x. "frame segment descriptor"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "a descriptor for a frame segment."

#### y. "data value"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "a value of bit(s) of data."

#### z. "first logic"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "first circuits and/or programming."

#### aa. "read and process data in the identified packets from the buffer"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "read and process data in the identified packets from the buffer."

#### bb. "second logic"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "second circuits and/or programming."

#### cc. "variant formats"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "varying arrangements of packet information other than a destination MAC address."

## dd. "means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to

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# the host processor responsive to a comparison of the counter and the alterable storage location"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,307,459, such "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "comparator 213" outputs data to "RCV COMPLETE control block 210" (see fig. 14, col. 31, ln. 41), which generates an indication signal (see col 31, ln. 41-49); "EARLY INDICATION LATCH block 512" (see col. 38, ln. 51-55); "early xmit complete block" (see col. 39, ln 57); and "AND gate 616" (see fig. 31; col. 40, ln. 46).

ee. "transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communication medium"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "transmit logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "network adapter 6" (see fig. 1; col. 4, ln. 2-4, 16-17); "transmit logic 39" (see fig. 2; col. 4, ln. 38); "network adapter 6" (see fig. 1; col. 4, ln. 2-4, 16-17); "transmit DMA module 67" (see figs. 4, 4A; col. 9, ln. 13-44); and "Ethernet transmitter module 66" (see fig.4; col. 9, ln. 45-51).

ff. "underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition"

In light of his review of the patent, prosecution history, and specification, in

gg.

connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "underrun control logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "logic" (see col. 2, ln. 30); "host interface logic" (see fig. 2; col. 4, ln. 57); an "underrun detector" (see fig. 18, col. 28, ln. 54); and "XMIT FAILURE register" (see col. 19, ln.14-38).

"means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41, 67).

In addition, while the particular limitation of this element that requires that these means be coupled to the buffer memory and include a host system alterable threshold store are not governed by 35 U.S.C. § 112 ¶ 6, such limitations are disclosed in connection with such means as "threshold logic 36" (see fig. 2; col. 4, ln. 30-31, 40-41), coupled to a threshold store which "in a preferred system, is dynamically programmable by the host computer 30." (see fig. 2; col. 4, ln. 46-47).

# hh. "data transfer circuitry, having a host system interface, for transferring data of frames to the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "data transfer circuitry" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "line 35" (see fig. 2; col. 4, ln. 30).

ii. "logic, coupled to the buffer memory, which monitors the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "early transmit logic 6A" (see fig. 1; col. 4, ln. 11); "download DMA logic 58" (see figs. 4, 4A; col. 23, ln. 22); "11 bit counter 300" (see fig. 11; col. 23, ln. 30); and "download bytesResidentValue" (see fig. 11; col. 24, ln. 9).

jj. "logic, responsive to the threshold determination of the logic which monitors the transferring of data to the buffer memory, which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame to the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61);

"download compare block 321" (see fig. 12; col. 24, ln. 61-62); "immediate data comparator 322" (see fig. 12; col. 24, ln. 64-65); and "data available control block 323" (see fig. 12; col. 24, ln. 67-68).

kk. "logic to transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types so that packets having a particular packet type are transferred out of the order of receipt, relative to packets having another packet type"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6. Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 6,327,625, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "packet filter 14" (see fig. 1; col. 4, ln. 13); "FIFO(s) 13" (see fig. 1; col. 4, ln. 2-5, 14); "frame start header 16" (see fig. 1; col. 4, ln. 15); "frame start header 17" (see fig. 1; col. 4, ln. 18); "top packet data 18" (see fig. 1; col. 4, ln. 18); "**IPsec queue 20**" (see fig. 1; col. 4, ln. 21); "**priority queue 21**" (see fig. 1; col. 4, ln. 21-22); "packet download/receive control block 22" (see fig. 1; col. 4, ln. 22-23); "IPsec packet processing resources 23" (see fig. 1; col. 4, ln. 25); "packet upload/transmit control logic 24" (see fig. 1; col. 4, ln. 26); "out of order packet transfer control block 25" (see fig. 1; col. 4, ln. 28); "logic 26" (see fig. 1; col. 4, ln. 29); "logic 27" (see fig. 1; col. 4, ln. 30); "memory arbitration logic 28" (see fig. 1; col. 4, ln. 34-35); "multiplexer 29" (see fig. 1; col. 4, ln. 35); "idle state 100" (see fig. 3; col. 5, ln. 10); "state 101" (see fig. 3; col. 5, ln. 12); "state 102" (see fig. 3; col. 5, ln. 14); "branch 103" (see fig. 3; col. 5, ln. 20); "branch 104" (see fig. 3; col. 5, ln. 21); "branch 105" (see fig. 3; col. 5, ln. 22); "state 106" (see fig. 3; col. 5, ln. 24); "state 107" (see fig. 3; col. 5, ln. 29); "state 108" (see fig. 3; col. 5, ln. 32); "state 120" (see fig. 4; col. 6, ln. 32); "state 121" (see fig. 4; col. 6, ln. 38); "state 122" (see fig. 4; col. 6, ln. 46);

"state 123" (see fig. 4; col. 6, ln. 49); "state 124" (see fig. 4; col. 6, ln. 54); "packet transmit/upload logic 24" (see fig. 5; col. 7, ln 16); "idle state 200" (see fig. 5; col. 7, ln 17-18); "state 201" (see fig. 5; col. 7, ln 19); "path 202" (see fig. 5; col. 7, ln 25); "align pointer state 203" (see fig. 5; col. 7, ln 25); "branch 204" (see fig. 5; col. 7, ln 25); "state 205" (see fig. 5; col. 7, ln 26); "data transfer state 206" (see fig. 5; col. 7, ln 29); "branch 207" (see fig. 5; col. 7, ln 50); "retransmit state 208" (see fig. 5; col. 7, ln 51); "branch 209" (see fig. 5; col. 7, ln 55); "flush state 210" (see fig. 5; col. 7, ln 57); "branch 211" (see fig. 5; col. 7, ln 62); "transfer complete state 212" (see fig. 5; col. 7, ln 62-63); and "resources 830" (see fig. 8; col. 13, ln. 48).

ll. "second logic coupled with the buffer, and responsive to the packet filter to read and process data in the identified packets from the buffer, and to produce a data value dependent on contents of the packet prior to transfer of the identified packets to the second port by the first logic"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 6,570,884, such "second logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "hardware filtering logic 15" (see fig. 1; col. 4, ln. 16); "embedded processor 14" (see fig. 1; col. 4, ln. 15-16); "line 18" (see fig. 1; col. 4, ln. 26); "embedded processor 118" (see fig. 2; col. 5, ln. 8); "pattern match modules, modules 203, 204, 205 and 206" (see fig. 3; col. 5, ln. 43); "packet classify unit 210" (see fig. 3; col. 5, ln. 44); "receive FIFO control logic 218" (see fig. 3; col. 6, ln. 29); "processor 220" (see fig. 3; col. 6, ln. 36); "block 300" (see fig. 4; col. 6, ln. 45); "block 301" (see fig. 4; col. 6, ln. 47-48); "block 302" (see fig. 4; col. 6, ln. 49); "block 303" (see fig. 4; col. 6, ln. 50); "block 304" (see fig. 4; col. 6, ln. 52); "block 305" (see fig. 4; col. 6, ln. 54); "block 306" (see fig. 4; col. 6, ln. 55); "block 400" (see fig. 5; col. 6, ln. 61); "block 41" (see col.

6, ln. 63); "block 401" (see fig. 5); "block 402" (see fig. 5; col. 6, ln. 64); "block 403" (see fig. 5; col. 7, ln. 2); "block 404" (see fig. 5; col. 7, ln. 5); "block 405" (see fig. 5; col. 7, ln. 7); "block 406" (see fig. 5; col. 7, ln. 8); "ARM7 processor" (col. 9, ln. 23); and "general purpose processor module" (see col. 11, ln. 29).

# mm. "means for comparing the counter to the threshold value in the alterable storage location"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,307,459, such "means for comparing" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "logic block 219" (see fig. 14; col. 32, ln. 3); "comparator 213" (see fig. 14; col. 32, ln. 25-26); "comparator 224" (see fig. 14; col. 32, ln. 46); "comparator 318" (see fig. 21; col. 36, ln. 15); "comparator 333" (fig. 23; col. 37, ln. 40); "THRESHOLD COMPARE block 511" (see fig. 24, 26; col. 38, ln. 42, 44); "comparator 517" (see fig. 26; col. 38, ln. 2-5); "comparator 615" (see fig. 31; col. 40, ln. 41-45).

#### nn. "means ... for transferring [data]"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for transferring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "host interface logic 31" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "download DMA module 58" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "XMIT AREA register" (see col. 18, ln. 6-10).

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#### "means, having a host system interface, for transferring data of 00. frames to the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for transferring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "host interface logic 31" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "download DMA module 58" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10).

#### "means ... for monitoring [the transferring of data]" pp.

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "threshold logic 36" (see fig. 2; col. 4, ln. 30-31, 40-41); "early transmit logic 6A" (see fig. 1; col. 4, ln. 11); "download DMA logic 58" (see figs. 4, 4A; col. 23, ln. 22); "11 bit counter 300" (see fig. 11; col. 23, ln. 30); and "download bytesResidentValue" (see fig. 11; col. 24, ln. 9).

#### "means ... for initiating [transmission]" qq.

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for initiating" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "transmit logic 39" (see fig. 2; col. 4, ln. 37-38); "start threshold register 320" (see fig. 12; col.

24, ln. 60-61); "download compare block 321" (see fig. 12; col. 24, ln. 61-62); "immediate data comparator 322" (see fig. 12; col. 24, ln. 64-65); and "data available control block 323" (see fig. 12; col. 24, ln. 67-68).

rr. "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "transmit logic 39" (see fig. 2; col. 4, ln. 37-38); "start threshold register 320" (see fig. 12; col. 24, ln. 60-61); "download compare block 321" (see fig. 12; col. 24, ln. 61-62); "immediate data comparator 322" (see fig. 12; col. 24, ln. 64-65); and "data available control block 323" (see fig. 12; col. 24, ln. 67-68).

#### ss. "[host interface] means ... for transferring [data]"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "host interface logic 31" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "download DMA module 58" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "XMIT AREA register" (see col. 18, ln. 6-10).

tt. "host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "data transfer circuitry" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "host interface logic 31" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "download DMA module 58" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "XMIT AREA register" (see col. 18, ln. 6-10).

uu. "means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "threshold logic 36" (see fig. 2; col. 4, ln. 30-31, 40-41); "early transmit logic 6A" (see fig. 1; col. 4, ln. 11); "download DMA logic 58" (see figs. 4, 4A; col. 23, ln. 22); "11 bit counter 300" (see fig. 11; col. 23, ln. 30); and "download bytesResidentValue" (see fig. 11; col. 24, ln. 9).

vv. "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C.  $\S$  112  $\P$  6, Dr.

Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for initiating" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "transmit logic 39" (see fig. 2; col. 4, ln. 37-38); "start threshold register 320" (see fig. 12; col. 24, ln. 60-61); "download compare block 321" (see fig. 12; col. 24, ln. 61-62); "immediate data comparator 322" (see fig. 12; col. 24, ln. 64-65); and "data available control block 323" (see fig. 12; col. 24, ln. 67-68).

#### ww. "[network interface] means ... for transferring [data]"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "network interface means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "transmit logic 39" (see fig. 2; col. 4, ln. 38); "transmit DMA module 67" (see figs. 4, 4A; col. 9, ln. 13-44); "Ethernet transmitter module 66" (see fig.4; col. 9, ln. 45-51); "Ethernet receiver module 62" (see fig.4; col. 9, ln. 53-59); "receive DMA module 63" (see figs. 4, 4A; col. 9, ln. 60-col. 10, ln. 12); and "upload DMA module 57" (see figs. 4, 4A; col. 10, ln. 13-37).

xx. "network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "network interface means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "network adapter 6" (see fig. 1; col. 4, ln. 2-4, 16-17); "transmit DMA module 67" (see figs. 4,

4A; col. 9, ln. 13-44); "Ethernet transmitter module 66" (see fig.4; col. 9, ln. 45-51); "Ethernet receiver module 62" (see fig.4; col. 9, ln. 53-59); "receive DMA module 63" (see figs. 4, 4A; col. 9, ln. 60-col. 10, ln. 12); and "upload DMA module 57" (see figs. 4, 4A; col. 10, ln. 13-37).

yy. "[control] means ... for posting [status information]"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for posting" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "logic" (see col. 2, ln. 30); "host interface logic" (see fig. 2; col. 4, ln. 57); an "underrun detector" (see fig. 18, col. 28, ln. 54); and "XMIT FAILURE register" (see col. 19, ln.14-38).

zz. "control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for posting" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "logic" (see col. 2, ln. 30); "host interface logic" (see fig. 2; col. 4, ln. 57); an "underrun detector" (see fig. 18, col. 28, ln. 54); and "XMIT FAILURE register" (see col. 19, ln.14-38).

aaa. "first logic coupled with the buffer and the second port, to transfer packets from the buffer to the second port"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. §  $112 \, \P \, 6$ , Dr.

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Mitzenmacher will assert that, as it appears in U.S. Patent No. 6,570,884, such "first logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**upload engine 116**" (see fig. 2) and "**load engine 116**" (see col. 4, ln. 64-65).

#### C. CONCLUSION

Dr. Mitzenmacher reserves the right to respond to any opinions put forth by Realtek Semiconductor Corp. or D-Link Systems Inc. in expert reports, during deposition, trial or otherwise, as well as any further documents, evidence or information regarding claims construction and to supplement this statement accordingly.

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**EXHIBIT B** 

SUMMARY OF TESTIMONY OF DR. IZHAK RUBIN IN SUPPORT OF REALTEK'S POSITIONS SET FORTH IN THE JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT PURSUANT TO PATENT LOCAL RULE 4-3

#### **QUALIFICATIONS** A.

Dr. Izhak Rubin received his Bachelor of Science and Master of Science degrees from the Technion – Israel Institute of Technology, Haifa, Israel, in 1964 and 1968, respectively, and his Ph.D. degree from Princeton University, Princeton, NJ, in 1970, all in Electrical Engineering. During 1964-1967, he served as a Communications Engineer and Officer in the Israeli Signal Corps. In 1967-1968, he worked as an Electronics and C3 Engineer in the Israel Aircraft Industries. Since 1970, he has been on the faculty of the University of California, Los Angeles ("UCLA"), School of Engineering and Applied Science, where he is currently a Professor in the Electrical Engineering Department.

Dr. Rubin has had extensive research, publications, consulting, and industrial experience in the design and analysis of commercial and military computer communications and telecommunications systems and networks. At UCLA, he is leading a large research group. He also serves as President of IRI Computer Communications Corporation, a company engaged in software development and consulting services.

During 1979-1980, Dr. Rubin served as Acting Chief Scientist of the Xerox Telecommunications Network. He served as co-chairman of the 1981 IEEE International Symposium on Information Theory; as program chairman of the 1984 NSF-UCLA workshop on Personal Communications; as program chairman for the 1987 IEEE INFOCOM conference; and as program co-chair of the IEEE 1993 workshop on Local and Metropolitan Area networks. Dr. Rubin is a Fellow of Institute of Electrical and Electronics Engineers ("IEEE"), a prestigious and international professional organization, the most distinguished membership grade bestowed by the IEEE and awarded only to a limited number of its distinguished members. He has been serving as an editor of the IEEE Transactions on Communications, of the ACM/Baltzer journal on Wireless Networks, of the Optical Networks magazine, of the Photonic Network Communications journal, and of the Communications Systems journal. He has contributed chapters to texts on telecommunications systems and networks.

B. GENERAL TESTIMONY

Dr. Rubin may be called to testify as Realtek's expert regarding the general purpose and use of network interface cards or controller chips and Ethernet networking technology, as well as the products involved the patents-in-suit. He may also testify as to the level of experience, knowledge, and skill typical of a person having ordinary skill in those arts concerned with the technology disclosed in the patents-in-suit and how the terms proposed collectively by both sides in this action for construction are used by a person having ordinary skill in the art, and specifically how such a person would interpret such terms in the context of the respective specifications, claims, and prosecution histories of the patents-in-suit. Dr. Rubin may also testify as to the structure(s), act(s), and/or material(s), and equivalents or lack thereof, disclosed in the respective specifications of the patents-in-suit or known to a person having ordinary skill in the art for each claim element found by the court to be governed by 35 U.S.C. § 112(6).

#### C. TESTIMONY ON CLAIM CONSTRUCTION

Dr. Rubin may provide written or oral testimony on the following matters:

1. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,307,459, to mean "storage location whose value is dynamically changeable."

- 2. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the terms "buffer" and "buffer memory," as each appears in claim 1 of U.S. Patent No. 5,307,459, claims 1, 10, and 21 of U.S. Patent No. 5,434,872, and claims 1, 9, 21, 28, 39, and 47 of U.S. Patent No. 5,732,094, to mean "a memory that (1) stores frame data such that the frame data can be retrieved independently of the order in which the frame data were stored and the frame data can always be retained and reused and can be accessed by the host system; and (2) is not a first-in-first-out (FIFO) system."
- 3. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "indication signal," as it appears in claim 1 of U.S. Patent No. 5,307,459, to mean "a signal that is not an interrupt, but may be used by the host system to generate an interrupt."
- 4. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "logic," as it appears in claims 1 and 21 of U.S. Patent No. 5,434,872; claim 1 of U.S. Patent No. 5,307,459; to mean "a device," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.
- 5. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "threshold value," as it appears in claim 1 of U.S. Patent No. 5,307,459, claim 10 of U.S. Patent No. 5,434,872, and claim 47 of U.S. Patent No. 5,732, 094, to mean "a number corresponding to a level of data required for some process to take place."
- 6. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "falls behind," as it appears in claim 1 of U.S.

Patent No. 5,434,872, to mean "a condition in which the transferring of data by the host interface falls behind the transferring of data by a transmit logic."

- 7. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "a condition in which the means for transferring falls behind the transmit logic," as it appears in claim 1 of U.S. Patent No. 5,434,872, to mean "a condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic."
- 8. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "underrun" and "falls behind" as each appears in claim 1 of U.S. No. 5,434,872 and claim 21 of U.S. Patent No. 5,732,094, to have the same meaning as "falls behind," which means "a condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic."
- 9. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "underrun control logic," as it appears in claim 1 of U.S. Patent No. 5,434,872, to mean "device for controlling underrun," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.
- 10. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "bad frame signal," as it appears in claim 1 of U.S. No. 5,434,872 and claim 21 of U.S. Patent No. 5,732,094, to mean "a signal indicating that a frame is bad."

- 11. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "feedback," as it appears in claim 10 of U.S. No. 5,434,872 and claims 21 and 47 of U.S. Patent No. 5,732,094, to mean "information from output that is returned to input."
- 12. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "optimizing the threshold," as it appears in claim 10 of U.S. No. 5,434,872 and claim 21 of U.S. Patent No. 5,732,094, to mean "dynamically changing the threshold value by the host system to make it as perfect, effective, or functional as possible."
- 13. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "threshold amount of data," as it appears in claim 21 of U.S. Patent No. 5,732,094, to mean "the amount of data required for some process to take place."
- 14. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "altering the threshold," as it appears in claim 47 of U.S. Patent No. 5,732,094, to mean "dynamically changing the threshold."
- 15. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term "logic", as it appears in many claimed elements of claims 1 and 21 of U.S. Patent No. 5,434,872 and claim 1 of U.S. Patent No. 5,307,459, as lacking suggestion or indication of specific structure.

- 16. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term "underrun control logic," as it appears in claim 1 of U.S. Patent No. 5,434,872, as lacking suggestion or indication of specific structure.
- In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Figs. 12a-18 receive threshold logic; Figs. 19-23 transfer threshold logic; Figs 24-28 download transmit threshold logic; Figs 29-34 transmit threshold logic.
- In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communication medium," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 transmit MAC Logic 39; Fig. 3 network interface processor 14; Fig. 4 RAM interface 50, transmit DMA 67, Ethernet transmitter 66; Fig. 4A transmit DMA 67; Fig. 5 transmit DMA logic 109, transceiver 105; Fig. 7 transmit descriptors; Fig. 8 transmit descriptor data structure; Fig. 9 transmit descriptor ring buffer 152, transmit DMA logic 155; Fig. 12 data available control block 323;

Fig. 17 – state machine elements 370, 371, 372, 373; Fig. 18 – transmit data path 400, paths 401, 402, MUX 410, transmit control logic 411.

- In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Figs. 12a-18 receive threshold logic, Figs. 19-23 transfer threshold logic, Figs 24-28 download transmit threshold logic, Figs. 29-34 transmit threshold logic.
- 20. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 18 CRC 404, exclusive OR gate 407, MUX 410, transmit control logic 411, underrun detector 413.
- 21. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes

to testify that the term, "means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory," as it appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – threshold logic 36, threshold store 43; Fig. 3 – RAM 15; Fig. 5 – transmit descriptor and download DMA logic 107; Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304, and D-type flip-flops 305, 206; Fig. 12 – start threshold register 320, download compare clock 321, and immediate data comparator 322; Fig. 13 – threshold registers 330, 331, and threshold valid register 332; Fig. 14 – threshold value state diagram elements 335-37; Fig. 15 – comparator 340, AND gate 341, comparator 342; Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355, comparator 357.

22. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "data transfer circuitry, having a host system interface, for transferring data of frames to the buffer memory," as it appears in claim 21 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – host interface 31, bus 2; Fig. 3 – network interface processor 14, bus 13; Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, upload DMA 57, download DMA module 58; Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3.0]; Fig. 5 – host interface logic 102, transmit descriptor logic, download DMA logic 107; Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152; Fig. 11 – adder 308, MUX 309, subtractor 310, register 311.

- 23. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "logic, coupled to the buffer memory, which monitors the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory," as it appears in claim 21 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Figs. 11-12 elements 300, 302, 303, 304, 305, 306, 307, 308, 309 310, 311, 320, 321, 322, and 323; Fig. 16 elements 350, 351, 352, 353, 354, 355, 356, and 357.
- 24. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "logic, responsive to the threshold determination of the logic which monitors the transferring of data to the buffer memory, which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame to the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory," as it appears in claim 21 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 threshold logic 36, threshold store 43; Fig. 3 RAM 15; Fig. 5 transmit descriptor and download DMA logic 107; Fig. 11 counter 300, AND Gate 301, delay circuit 302, adder 304 and D-type flip-flops 305, 306; Fig. 12 start threshold register 320, download compare block 321, immediate data comparator 322; Fig. 13 threshold registers 330, 331, and threshold valid register 332; Fig. 14 threshold valid state diagram elements 335-337; Fig. 15 –

comparator 340, AND gate 341, comparator 342; Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355 comparator 357.

- 25. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means for comparing the counter to the threshold value in the alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2, includes without limitation threshold logic 10, alterable storage location 10a, host processor 5, network adaptor 3; Figs. 12a-18, includes without limitation register 221, counter 216, logic block 218, comparator 213, register 223, comparator 224, logic block 222; Figs. 19-23, includes without limitation. adder 317, comparator 318; Figs. 24-28, includes without limitation comparator 333; Figs. 29-34, includes without limitation, adder 614, comparator 615.
- 26. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "network interface logic for transferring the data frame between the network transceiver and the buffer memory," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 network interface logic 11; Fig. 4 receive DMA 63, Transmit DMA 67; Fig. 5 network interface logic 104; Fig. 9 transmit DMA logic 155; Fig. 11 DMA logic 302; Figs. 14-18 receive DMA Block; Figs. 29-34 transmit DMA Block.

- 27. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "host interface logic for transferring the data frame between the host system and the buffer memory," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 host interface logic 11; Fig. 4 download DMA 58, upload DMA 57; Fig. 5 host interface logic 102; Fig. 9 host interface logic including 150 and 151; Fig. 11 upload DMA logic 300 and preview logic 301; Figs. 19-23 upload DMA Block; Figs. 24-28 download DMA Block.
- 28. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "means ... for transferring [data]" and "means, having a host system interface, for transferring data of frames to the buffer memory," as each of them appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 1 bus 2; Fig. 2 host interface 31, bus 2; Fig. 3 network interface processor 14, bus 13; Fig. 4 RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, download DMA module 57; Fig. 4A download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3:0]; Fig. 5 host interface logic 102, transmit descriptor and download DMA logic 107; Fig. 9 host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152.
- 29. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the

extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "means ... for initiating [transmission]" and "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer," as each appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 1 – early transmit logic 6A; Fig. 2 – transmit MAC logic; Fig. 3 – network interface processor; Fig. 4 & 4A – transmit DMA 67; Fig. 5 – network interface logic 104; Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155; Fig. 12 – data available control block 323; Fig. 17 – state machine elements 370, 371, 372, 373; Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.

30. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "[host interface] means ... for transferring [data]" and "host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory," as each appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 2 – host interface 31, bus 2; Fig. 3 – network interface processor 14, bus 13; Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, upload DMA 57, download DMA module 58; Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3.0]; Fig. 5 – host interface logic 102, transmit descriptor logic and download DMA logic 107; Fig. 6 – transmit area; Fig. 7 – transmit descriptors; Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152; Fig. 11 – adder 308, MUX 309, subtractor 310, and register 311.

- 31. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "means ... for monitoring [the transferring of data]" and "means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory," as each appears in claim 1 and claim 10, respectively, of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 2 – threshold logic 36, threshold store 43; Fig. 3 – RAM 15; Fig. 5 – transmit descriptor and download DMA logic 107; Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304, and D-type flip-flops 305, 206; Fig. 12 – start threshold register 320, download compare clock 321, and immediate data comparator 322; Fig. 13 – threshold registers 330, 331, and threshold valid register 332; Fig. 14 – threshold value state diagram elements 335-37; Fig. 15 – comparator 340, AND gate 341, comparator 342; Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355, comparator 357.
- 32. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 1 early transmit logic 6A; Fig. 9 transmit descriptor ring buffer 152, transmit DMA logic 155;

Fig. 12 – data available control block 323; Fig. 17 – state machine elements 370, 371, 372, 373; Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.

- 33. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "[network interface] means ... for transferring [data]" and "network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission," as each appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 3 network interface processor 14, encoder/decoder 19; Fig. 4 cycle arbiter 56, interrupt controller 60, Ethernet transmitter 66, and transmit DMA 67; Fig. 4A transmit DMA 67; Fig. 5 transmit DMA logic 109; Fig. 7 transmit descriptors; Fig. 9 transmit descriptor ring buffer 152, transmit DMA logic 155; Fig. 18 transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.
- 34. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "[control] means ... for posting [status information]" and "control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value," as each appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 18 transmit control logic 411 and underrun detector 413.

## II. SUMMARY OF TESTIMONY OF NICK BAMBOS IN SUPPORT OF REALTEK'S POSITIONS SET FORTH IN THE JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT PURSUANT TO PATENT LOCAL RULE 4-3

## A. QUALIFICATIONS

Dr. Nick Bambos received his Ph.D. in Electrical Engineering and Computer Sciences in 1989, his M.S. degree in EECS in 1987, and his M.A. degree in Mathematics in 1989 all from the University of California at Berkeley.

Dr. Bambos is now a professor at Stanford University, having a joint appointment in the Department of Electrical Engineering and the Department of Management Science & Engineering. He heads the Network Architecture and Performance Engineering research group, comprised of doctoral students and research visitors conducting research in wireless network architectures, the Internet infrastructure, network security/reliability and operations management. His current research interests include high-reliability/security information systems, autonomic computing, and management of IP/wireless network infrastructures.

Dr. Bambos has held the Cisco Systems Faculty Development Chair in computer networking at Stanford from 1999 to 2003. He has also won the IBM Faculty Award in 2002 for high-impact research in performance engineering of computer systems and networks, as well as the Griffin Award in 1997. He has been the Morgenthaler Faculty Scholar at Stanford from 1996 to 1999. Dr. Bambos has also received the National Young Investigator Award in 1992 from the National Science Foundation (NSF) for research in computer networks and distributed computing architectures, as well as the NSF Research Initiation Award in 1990 for studies in performance modeling of computer systems.

Dr. Bambos has been a U.C. Regents Fellow, a David Gale Fellow, and an Earl Anthony Fellow, and is now on the Editorial Boards of several research journals and serves on various international technical committees and review panels for networking research and

information technologies.

## B. GENERAL TESTIMONY

Dr. Bambos may be called to testify as Realtek's expert regarding the general purpose and use of network interface cards and Ethernet networking technology, as well as the specific network interface cards of the patents-in-suit. He may also testify as to the level of experience, knowledge, and skill typical of a person having ordinary skill in those arts concerned with the technology disclosed in the patents-in-suit and how the terms proposed collectively by both sides in this action for construction are used by a person having ordinary skill in the art, and specifically how such a person would interpret such terms in the context of the respective specifications, claims, and prosecution histories of the patents-in-suit. Dr. Bambos may also testify as to the structure(s), act(s), and/or material(s), and equivalents or lack thereof, disclosed in the respective specifications of the patents-in-suit or known to a person having ordinary skill in the art for each claim element found by the court to be governed by 35 U.S.C. § 112(6).

## C. TESTIMONY ON CLAIM CONSTRUCTION

Dr. Bambos is also expected to provide written or oral testimony on the following matters:

- 1. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "buffer," as it appears in claims 23 of U.S. Patent No. 6,327,625 and claim 1 of U.S. Patent No. 6,570,884, to mean "a temporary storage area in random access memory where the NIC or computer stores information."
- 2. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "logic," as it appears in claim 23 of U.S. Patent No. 6,327,625 and claim 1 of U.S. Patent No. 6,570,884 to mean "a device," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.

- 3. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "order of receipt," as it appears in claim 23 of U.S. Patent No. 6,327,625, to mean "the order in which the packets are received by the buffer."
- 4. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "packet types," as it appears in claim 23 of U.S. Patent No. 6,327,625, to mean "packets with different formats or priorities."
- 5. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types," as it appears in claim 23 of U.S. Patent No. 6,327,625, to mean "the order in which packets are transferred out of the buffer is based upon the order in which the packets were received by the buffer and the types of the packets stored in the buffer."
- 6. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "data download circuit," as it appears in claim 26 of U.S. Patent No. 6,526,446, to mean "the circuitry that downloads data corresponding to the frame segment descriptor."
- 7. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "descriptor signal," as it appears in claim 26 of U.S. Patent No. 6,526,446, to mean "a signal indicating where the corresponding data is in the host memory."
- 8. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "frame segment descriptor," as it appears in

claim 26 of U.S. Patent No. 6,526,446, to mean "a descriptor identifying where the corresponding frame segment is in the host memory."

- 9. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "first logic," as it appears in claim 1 of U.S. Patent No. 6,570,884 to mean "first device," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.
- 10. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "read and process data in the identified packets from the buffer," as it appears in claim 1 of U.S. Patent No. 6,570,884, to mean "read and process data in the identified packets while the packets are in the buffer."
- In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "second logic," as it appears in claim 1 of U.S. Patent No. 6,570,884 to mean "second device," should the Court determine that the term should not be construed under 35 U.S. C.  $\S$  112  $\P$  6.
- 12. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "variant formats," as it appears in claim 1 of U.S. Patent No. 6,570,884, to mean "differing formats."